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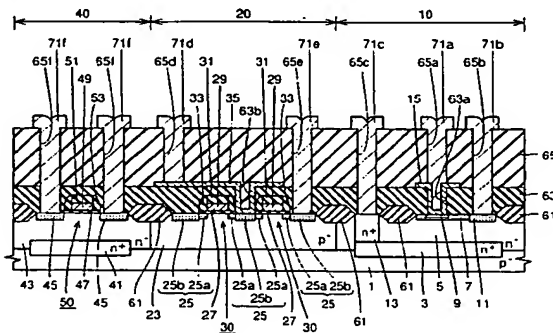
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Semiconductor bipolar device and method of manufacturing the same.

An  $n^+$  buried layer (3) is formed on a surface of  $p^-$  semiconductor substrate (1). An  $n^-$  epitaxial growth layer (5) and an  $n^+$  diffusion layer (13) are formed on a surface of  $n^+$  buried layer (3). A  $p^-$  base region (7) and  $p^+$  external base region (11) adjoining to each other are formed on a surface of  $n^-$  epitaxial growth layer (5). An  $n^+$  emitter region (9) is formed at a surface of  $p^-$  base region (7). An emitter electrode (15) is formed adjacently to  $n^+$  emitter region (9). Emitter electrode (15) is made of polycrystalline silicon doped with phosphorus at a concentration from  $1 \times 10^{20} \text{ cm}^{-3}$  to  $6 \times 10^{20} \text{ cm}^{-3}$ .

FIG. 1



## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a semiconductor device and a method of manufacturing the same, and in particular to a semiconductor device including bipolar transistors and a method of manufacturing the same.

### Description of the Background Art

In recent years, performance of industrial equipments such as computers has been remarkably improved. A Bi-CMOS (Bipolar Complementary Metal Oxide Semiconductor) structure in which a bipolar transistor and a CMOS transistor are formed on the same semiconductor substrate has attracted the attention from the aspect of complying with the aforementioned remarkable performance. The Bi-CMOS structure can achieve high-speed operation, i.e., feature of the bipolar transistor, as well as high integration and low power consumption, i.e., feature of the CMOS transistor.

A conventional semiconductor device will be described below particularly in connection with the structure of Bi-CMOS structure including bipolar transistors.

Fig. 62 is a cross section schematically showing a structure of the conventional semiconductor device. Referring to Fig. 62, the Bi-CMOS structure has a bipolar transistor region 510, an nMOS transistor region 520 and a pMOS transistor region 540.

In bipolar transistor region 510, an  $n^+$  buried layer 503 is formed on a surface of a  $p^-$  semiconductor substrate 501. An  $n^-$  epitaxial growth layer 505 and an  $n^+$  diffusion layer 513 for leading out a collector are formed on the surface of  $n^+$  buried layer 503.

A  $p^-$  base region 507 and a  $p^+$  external base region 511 adjoining to each other are formed on the surface of  $n^-$  epitaxial growth layer 505. An  $n^+$  emitter region 509 is formed on  $p^-$  base region 507.

A first interlayer insulating film 563 is formed over the surface of bipolar transistor 510. First interlayer insulating film 563 is provided with a contact hole 563a reaching  $n^+$  emitter region 509. An emitter electrode 515 is formed on the surface of first interlayer insulating film 563 and is in contact with  $n^+$  emitter region 509 through contact hole 563a. Emitter electrode 515 is made of polycrystalline silicon doped with arsenic (As).

Emitter electrode 515 is covered with a second interlayer insulating film 565 formed on the surface of first interlayer insulating film 563. Second interlayer insulating film 565 is provided with a contact

hole 565a reaching emitter electrode 515. A conductive layer 571a is in contact with emitter electrode 515 through contact hole 565a.

First and second interlayer insulating films 563 and 565 are provided with contact holes 565b and 565c, which reach  $p^+$  external base region 511 and  $n^+$  diffusion layer 513, respectively. Conductive layers 571b and 571c are in contact with  $p^+$  external base region 511 and  $n^+$  diffusion region 513 through contact holes 565b and 565c, respectively.

In nMOS transistor region 520, a  $p^-$  well region 523 is formed on the surface of  $p^-$  semiconductor substrate 501. A plurality of nMOS transistors 530 are formed on the surface of  $p^-$  well region 523.

Each nMOS transistor 530 includes a pair of n-type source/drain regions 525, a gate oxide film 527 and a gate electrode 529.

Each pair of n-type source/drain regions 525 are formed on  $p^-$  well region 523 with a predetermined space between each other. n-type source/drain region 525 has an LDD (Lightly Doped Drain) structure formed of a relatively lightly doped  $n^-$  impurity region 525a and a relatively heavily doped  $n^+$  impurity region 525b. A gate electrode 529 is formed on a region between paired n-type source/drain regions 525 with a gate oxide film 527 therebetween.

nMOS transistor 530 is covered with first interlayer insulating film 563. First interlayer insulating film 563 is provided with an aperture 563b which reaches one of paired source/drain regions 525. An interconnection layer 535 is formed on first interlayer insulating film 563 and is in contact with n-type source/drain region 525 through aperture 563b. Interconnection layer 535 is made of polycrystalline silicon doped with arsenic.

The surface of interconnection layer 535 is covered with second interlayer insulating film 565, which is provided with a contact hole 565d reaching interconnection layer 535. A conductive layer 571d is in contact with interconnection layer 535 through contact hole 565d.

First and second interlayer insulating films 563 and 565 are provided with a contact hole 565e reaching n-type source/drain region 525. A conductive layer 571e is in contact with n-type source/drain region 525 through contact hole 565e.

In pMOS transistor region 540, an  $n^+$  buried layer 541 is formed on the surface of  $p^-$  semiconductor substrate 501. An  $n^-$  well region 543 is formed on the surface of  $n^+$  buried layer 541. A pMOS transistor 550 is formed on the surface of  $n^-$  well region 543.

pMOS transistor 550 has a pair of  $p^+$  source/drain regions 545, a gate oxide film 547 and a gate electrode 549.

A pair of  $p^+$  source/drain regions 545 are formed on the surface of  $n^-$  well region 543 with a

predetermined space between each other. Gate electrode 549 is formed on a region between paired p<sup>+</sup> source/drain regions 545 with a gate oxide film 547 therebetween.

pMOS transistor 550 is covered with first and second interlayer insulating films 563 and 565. First and second interlayer insulating films 563 and 565 are provided with contact holes 565f reaching paired p<sup>+</sup> source/drain regions 545. Conductive layers 571f are in contact with p<sup>+</sup> source/drain regions 545 through contact holes 565f.

Element isolating oxide films 561 are provided for electrically isolating regions 510, 520 and 540 and others from each other.

A method of manufacturing the conventional semiconductor device will be described below.

Figs. 63 to 83 are schematic cross sections showing a process of manufacturing the conventional semiconductor device in accordance with the order of process steps. Referring first to Fig. 63, a silicon oxide film 581 is formed on the whole surface of p<sup>-</sup> semiconductor substrate 501, for example, by thermal oxidation. Thereafter, silicon oxide film 581 is patterned into a predetermined configuration. Using silicon oxide film 581 thus patterned as a mask, impurity such as antimony (Sb) is implanted into p<sup>-</sup> semiconductor substrate 501. Then, heat treatment at about 1100°C is executed for about 2 hours, whereby n<sup>+</sup> layers 503a and 541a are formed on the surface of p<sup>-</sup> semiconductor substrate 501. Thereafter, silicon oxide film 581 is removed.

Referring to Fig. 64, n<sup>-</sup> epitaxial growth layer 505 is formed on the whole surface of p<sup>-</sup> semiconductor substrate 501. Thereby, such a structure is completed that n<sup>+</sup> buried layers 503 and 541 are buried between p<sup>-</sup> semiconductor substrate 501 and n<sup>-</sup> epitaxial growth layer 505.

Referring to Fig. 65, n-type impurity such as phosphorus (P) is introduced into n<sup>-</sup> epitaxial growth layer 543 located above n<sup>+</sup> buried layer 541 and then is diffused. Thereby, n<sup>-</sup> well region 543 is formed above n<sup>+</sup> buried layer 541. p-type impurity such as boron (B) is introduced into a predetermined region in n<sup>-</sup> epitaxial growth layer 505 and then is diffused. Thereby, p<sup>-</sup> well region 523 is formed.

Referring to Fig. 66, element isolating oxide films 561 are formed at predetermined regions, for example, by an LOCOS (Local Oxidation of Silicon) method.

Referring to Fig. 67, a silicon oxide film (SiO<sub>2</sub>) 583 and a silicon nitride film (Si<sub>3</sub>N<sub>4</sub>) 585, which have apertures at predetermined regions and are 300Å and 1000Å in thickness, respectively, are formed by deposition successively on the whole surface. Using silicon oxide film 583 and silicon nitride film 585 as a mask, the structure is exposed

to an atmosphere containing, e.g., POCl<sub>3</sub>. Thereby, phosphorus is diffused into n<sup>-</sup> epitaxial growth layer 505 to form n<sup>+</sup> diffusion layer 513 for leading the collector. Thereafter, silicon nitride film 585 and silicon oxide film 583 are successively removed.

Referring to Fig. 68, a thermal oxidation film 527a is formed on the whole surface by thermal oxidation. Then, an LPCVD (Low Pressure Chemical Vapor Deposition) method is used to form a polycrystalline silicon film 529a and a silicon oxide film 531a each having a thickness of about 2000Å by successive deposition. The silicon oxide film 531a and polycrystalline silicon film 529a are patterned into a predetermined configuration by photolithography and etching.

Referring to Fig. 69, gate electrodes 529 and 549 having the predetermined configuration are formed by the aforementioned patterning.

Referring to Fig. 70, photoresist 591a is applied to the whole surface, and then is exposed and developed. Thereby, a resist pattern 591a exposing the nMOS transistor region is formed. Using resist pattern 591a and gate electrode 529 as a mask, n-type impurity is implanted to form relatively lightly doped n<sup>-</sup> impurity region 525a on the surface of p<sup>-</sup> well region 523. Thereafter, resist pattern 591a is removed.

Referring to Fig. 71, a silicon oxide film 533a is formed over the whole surface. Thereafter, anisotropic etching is effected on silicon oxide film 533a.

Referring to Fig. 72, by the aforementioned anisotropic etching, side wall oxide films 533 and 553 covering side walls of gate electrodes 529 and 549 are formed. This anisotropic etching removes thin silicon oxide film 527a at a lower level, whereby gate oxide films 527 and 547 are formed.

Referring to Fig. 73, photoresist 591b is applied to the whole surface, and is exposed and developed. Thereby, resist pattern 591b exposing the nMOS transistor region is formed. Using resist pattern 591b, gate electrodes 529, and side wall oxide films 533 as a mask, n-type impurity is implanted. This implantation forms relatively heavily doped n<sup>+</sup> impurity regions 525b on the surface of p<sup>-</sup> well region. n<sup>-</sup> impurity regions 525a and n<sup>+</sup> impurity regions 525b form n-type source/drain regions 525 having a LDD structure. Thereby, nMOS transistors 530 are formed. Thereafter, resist pattern 591 is removed.

Referring to Fig. 74, photoresist 591c is applied to the whole surface, and is exposed and developed to form resist pattern 591c which exposes the pMOS transistor region and a predetermined region of the bipolar transistor. Using resist pattern 591c as a mask, p-type impurity is implanted into n<sup>-</sup> well region 543 and n<sup>-</sup> epitaxial growth layer 505. This implantation forms p<sup>+</sup> source/drain regions

545 at the pMOS transistor region and also forms p<sup>+</sup> external base region 511 at the bipolar transistor region. Thereby, pMOS transistor 550 is formed. Thereafter, resist pattern 591c is removed.

Referring to Fig. 75, photoresist 591d is applied to the whole surface, and is exposed and developed to form resist pattern 591d which exposes a predetermined region of the bipolar transistor. Using resist pattern 591d as a mask, p-type impurity is implanted into n<sup>-</sup> epitaxial growth layer 505. By this implantation and others, p<sup>-</sup> base region 507 adjoining to p<sup>+</sup> external base region 511 are formed. Thereafter, resist pattern 591d is removed.

Referring to Fig. 76, first interlayer insulating film 563 made of, e.g., a silicon oxide film is formed on the whole surface. The surface of first interlayer insulating film 563 has unevenness reflecting difference in level of lower layers.

Referring to Fig. 77, photoresist 591e is applied to the whole surface, and is exposed and developed to form resist pattern 591e having a predetermined configuration. Using this resist pattern 591e as a mask, processing such as RIE (Reactive Ion Etching) is effected on the first interlayer insulating film 563. In first interlayer insulating film 563, the aforementioned processing such as RIE forms emitter aperture 563a which partially exposes the surface of p<sup>-</sup> base region 507, and also forms aperture 563b which exposes n-type source/drain region 525. Thereafter, resist pattern 591e is removed.

Referring to Fig. 78, the LPCVD method is executed to form polycrystalline silicon film 515a on the whole surface of first interlayer insulating film 563.

Referring to Fig. 79, arsenic is implanted into the whole surface of polycrystalline silicon film 515a. Thereafter, RTA (Rapid Thermal Annealing) or the like is executed to effect high temperature thermal treatment thereon, for example, at a temperature of about 1050°C for about 30 seconds. Thereby, arsenic is uniformly diffused into doped polycrystalline silicon film 515b, and is also diffused into n<sup>-</sup> epitaxial growth layer 505, so that n<sup>+</sup> emitter region 509 is formed.

Referring to Fig. 80, doped polycrystalline silicon film 515b is patterned into a predetermined configuration by photolithography and etching. This forms emitter electrode 515 connected to n<sup>+</sup> emitter region 509 through emitter aperture 563a, and interconnection layer 535 connected to n-type source/drain region 525 through aperture 563b.

Referring to Fig. 81, second interlayer insulating film 565 is formed on the whole surface of first interlayer insulating film 563 to cover emitter electrode 515 and interconnection layer 535. Photoresist 591f is applied to the whole surface of second

interlayer insulating film 565, and is exposed and developed. Resist pattern 591f thus formed and having a predetermined configuration is used as a mask for effecting anisotropic etching. This etching forms contact holes 565a, 565b, 565c, 565d, 565e and 565f. Thereafter, resist pattern 591f is removed.

Referring to Fig. 82, conductive layers 571a, 571b, 571c, 571d, 571e and 571f are formed, which are in contact with conductive regions or others exposed at the bottoms through contact holes 565a, 565b, 565c, 565d, 565e and 565f, respectively.

In the conventional method of manufacturing the semiconductor device described above, it is necessary to carry out heat treatment by RTA in the process shown in Fig. 79. According to the RTA, wafer only is thermally processed at a high temperature by lamp heating. The heat treatment by the RTA is required because of the following reason.

In the conventional method of manufacturing the semiconductor device, emitter electrode 515 and interconnection layer 535 shown in Fig. 62 are formed by patterning the polycrystalline silicon film into which impurity is ion-implanted.

More specifically, at the process shown in Figs. 78 and 79, impurity is ion-implanted into polycrystalline silicon film 515a. The impurity is injected from above the substrate and perpendicularly into the substrate. Therefore, non-implanted regions in which impurity has not been implanted are formed along the side walls of aperture 563b and emitter aperture 563a in doped polycrystalline silicon film 515b within regions S<sub>1</sub> and S<sub>2</sub> in Fig. 79.

Fig. 83 is an enlarged fragmentary cross section showing region S<sub>1</sub> in Fig. 79 for explaining the fact that there is generated the non-implanted regions. Referring to Fig. 83, the side wall of aperture 563b has a height H<sub>2</sub> from the surface of p<sup>-</sup> well region 523. This height H<sub>2</sub> is much larger than a thickness T<sub>p</sub> of doped polycrystalline silicon film 515a. Therefore, it is very difficult to ion-implant the impurity into portions along the side walls.

In particular, in the MOS transistor region, a gate part portion must be formed on the substrate. Therefore, height H<sub>2</sub> of side wall of first interlayer insulating film 563 is large due to a height H<sub>1</sub> of the gate portion (i.e., gate oxide film 527, gate electrode 529 and insulating film 531). Meanwhile, in the bipolar transistor region, a gate electrode is not necessary. Therefore, height H<sub>2</sub> of side wall of aperture 563b formed in the MOS transistor region is larger than the height of side wall of emitter aperture formed in the bipolar transistor region within region S<sub>2</sub> in Fig. 79. As is apparent from the above, impurity is hardly implanted into the portion

of polycrystalline silicon film 515a along the high side wall of aperture 563b.

When the side wall has the non-implanted region, a so-called non-diffusion region 515a, i.e., region into which impurity is not diffused, is formed at the side wall of doped polycrystalline silicon film 563b as shown in Fig. 84, unless high temperature heat treatment such as RTA is not effected.

Interconnection layer 515b generally has the interconnection resistance as shown in Fig. 85. The interconnection resistance is represented as combination of resistances of portions other than that within aperture 563b (which will be referred to as "resistances of flat portions"), resistances of the side wall of aperture 563b and a resistance of a contact portion (boundary surface) between aperture 563b and source/drain region 525. Therefore, if non-diffusion region 515a is formed, the resistance of the side wall increases, so that the interconnection resistance of interconnection layer 515b locally increases.

In order to prevent increase of the interconnection resistance, it is necessary to uniformly diffuse the impurity for preventing generation of the non-diffusion region. Therefore, the high temperature heat treatment by RTA is required so as to uniformly diffuse the impurity up to the side wall of aperture 563b as shown in Fig. 84.

The conventional method of manufacturing the semiconductor device requires the heat treatment by RTA as described above.

Due to the heat treatment by RTA, the conventional semiconductor device and the method of manufacturing the same have such problems that (1) degree of integration cannot be improved and that (2) interconnection resistance of the emitter electrode and others can be reduced. These problems will be described below in greater detail.

#### (1) In connection with improvement of degree of integration

Elimination of the heat treatment is essential in order to improve the degree of integration and the performance of the conventional semiconductor device according to a scaling rule. The same is especially true with respect to the MOS transistor.

Referring to Fig. 86, the heat treatment by RTA is executed for uniform diffusion of impurity into doped polycrystalline silicon film 515b as described above. The high temperature heat treatment, however, causes  $n^+$  impurity region 525b to spread in a depth direction indicated by arrows  $J_1$  and a width direction indicated by arrows  $J_2$ . Thus, a so-called shallow junction cannot be formed.

In such case,  $n^+$  source/drain regions 525b spread as shown by dotted line in the figure, so that punch-through is likely to occur. Since  $n^-$

impurity regions 525a are taken into  $n^+$  impurity regions 525b, it is difficult to reduce a hot electron effect.

In order to achieve the high integration, a gate length  $L_{G1}$  of gate electrode 529 may be reduced, in which case a distance between adjoining  $n^+$  source/drain regions 525b decreases. Therefore, heat treatment by RTA will promote the disadvantageous punch-through and impair a characteristic relating to resistance against hot electrons. Therefore, gate length  $L_{G1}$  of gate electrode 529 cannot be reduced, which makes it difficult to improve the degree of integration. As described above, the conventional method of manufacturing the semiconductor device cannot sufficiently improve the degree of integration because it requires the high temperature heat treatment such as RTA.

#### (2) With respect to reduction of interconnection resistance of emitter electrode and others

Generally, if arsenic and phosphorus are introduced into polycrystalline silicon, segregation of arsenic at grain boundaries in the polycrystalline silicon is more likely than phosphorus. Therefore, if arsenic and phosphorus are individually introduced at the same concentration into the polycrystalline silicon, a concentration of carriers (activated impurity in grains) of arsenic would be lower than that of phosphorus by a degree corresponding to the segregation of arsenic at the grain boundaries.

Fig. 87 shows a relationship between an annealing temperature and a carrier concentration in the case where phosphorus and arsenic are individually introduced into polycrystalline silicon at a concentration of  $2 \times 10^{19} \text{ cm}^{-3}$ . As is seen from Fig. 87, in the case where arsenic and phosphorus are individually implanted to attain the same concentration, the concentration of carries of phosphorus is higher than that of arsenic regardless of the annealing temperature. If these are introduced to have the same concentration, therefore, phosphorus can achieve a lower resistance. From a viewpoint of the low resistance, therefore, polycrystalline silicon doped with phosphorus is more suitable to the interconnection layer than that doped with arsenic.

Fig. 88 shows a relationship between an impurity concentration and a resistivity when phosphorus and arsenic are individually introduced into polycrystalline silicon. In the case of arsenic shown in Fig. 88, the resistivity is saturated and will no longer lower when the concentration attains  $2 \times 10^{20} \text{ cm}^{-3}$  or more. Meanwhile, in the case of phosphorus, the resistivity lowers even at the concentration higher than the aforementioned value. As can be seen also from this result, polycrystalline silicon doped with phosphorus is more suitable to the interconnection layer than polycrystalline silicon

doped with arsenic from the viewpoint of low resistance.

However, phosphorus is diffused more rapidly than arsenic. Therefore, if polycrystalline silicon 515b were doped with phosphorus at the conventional manufacturing step shown in Fig. 79, and then RTA were effected to form emitter region 509 in Fig. 80, emitter region 509 would spread excessively, in which case an intended base width might not be obtained.

Fig. 89 shows a reason by which the intended base width cannot be obtained if the polycrystalline silicon is doped with phosphorus. Referring to Fig. 89, high temperature heat treatment promotes diffusion of phosphorus from emitter electrode 515 toward p<sup>-</sup> base region 507 in a direction indicated by arrow J. Thereby, n<sup>+</sup> emitter region 509 is formed deep, resulting in reduction of a width W<sub>2</sub> of p<sup>-</sup> base region 507 immediately under n<sup>+</sup> emitter region 509. If width W<sub>2</sub> of p<sup>-</sup> base region 507 is small, a collector-emitter breakdown voltage of the npn bipolar transistor decreases.

In view of the reduction of the breakdown voltage, it has been difficult to introduce phosphorus at a high concentration into emitter electrode 515. In the conventional semiconductor device, therefore, the phosphorus concentration cannot be larger than  $1 \times 10^{20} \text{ cm}^{-3}$  if phosphorus is introduced into emitter electrode 515. Although it is preferable to introduce phosphorus from the viewpoint of the interconnection resistance, the concentration of phosphorus cannot be high because of the aforementioned reason, so that it is impossible to reduce the interconnection resistance of emitter electrode 515 in the prior art.

Consequently, according to the conventional semiconductor device and the method of manufacturing the same, it is impossible to further reduce the overall interconnection resistance of the emitter electrode while maintaining a good breakdown voltage characteristic.

## SUMMARY OF THE INVENTION

An object of the invention is to provide a method of manufacturing a semiconductor device of which degree of integration can be easily improved.

Another object of the invention is to provide a semiconductor device, in which interconnection resistances of an emitter electrode and others are reduced, as well as a method of manufacturing the same.

A method of manufacturing a semiconductor device of the invention includes the following steps.

First, a collector impurity region of a first conductivity type is formed on a main surface of a semiconductor substrate. A base impurity region of

a second conductivity type is formed on the main surface of the semiconductor substrate within the collector impurity region. An emitter impurity region of the first conductivity type is formed at the main surface of the semiconductor substrate with the base impurity region. A vapor deposition method is carried out to form polycrystalline silicon which is doped with phosphorus and is in contact with the emitter impurity region.

According to the method of manufacturing the semiconductor device of the invention, the polycrystalline silicon doped with the phosphorus is formed by the vapor deposition method. Thus, the phosphorus is introduced into the polycrystalline silicon simultaneously with the formation thereof by the vapor deposition method. According to this method, the phosphorus is uniformly introduced into the polycrystalline silicon. Therefore, it is possible to eliminate a heat treatment at a high temperature by RTA which has been required for uniform diffusion of the impurity into the polycrystalline silicon. Owing to elimination of the heat treatment by the RTA, it is possible to prevent spreading of n<sup>+</sup> impurity region forming an LDD structure particularly in an MOS transistor. Therefore, it is possible to prevent problems such as punch through and deterioration of characteristics relating to a resistance against hot electrons in the MOS transistor. Accordingly, sizes of various portions such as a gate length of the MOS transistor can be reduced, which facilitates increase of a degree of integration.

Since it is possible to eliminate the heat treatment by RTA, it is naturally possible to prevent diffusion of impurity from an emitter electrode into a base impurity region, which may be caused during the heat treatment. Such a problem can also be prevented that the emitter impurity region is formed deep in the base impurity region due to the above diffusion and thereby a width of the base impurity region is reduced. Accordingly, even if a concentration of the phosphorus in the emitter electrode is increased, a collector-emitter breakdown voltage of a bipolar transistor does not deteriorate, and a good breakdown voltage characteristic can be maintained. Therefore, an interconnection resistance of the emitter electrode can be reduced while maintaining a good breakdown voltage characteristic.

A semiconductor device according to the invention includes a semiconductor substrate, a collector impurity region of a first conductivity type, a base impurity region of a second conductivity type, an emitter impurity region of the first conductivity type, and a conductive layer. The semiconductor substrate has a main surface. The collector impurity region of the first conductivity type is formed at the main surface of the semiconductor substrate.

The base impurity region of the second conductivity type is formed at the main surface of the semiconductor substrate within the base impurity region of the second conductivity type. The emitter impurity region of the first conductivity type is formed at the main surface of the semiconductor substrate with the base impurity region. The conductive layer is in contact with the emitter impurity region. The conductive layer contains polycrystalline silicon into which phosphorus is introduced at a concentration not less than  $1 \times 10^{20} \text{ cm}^{-3}$ .

The semiconductor device according to the above aspect of the invention, the concentration of the phosphorus can be increased. Therefore, the concentration of the phosphorus which is introduced substantially uniformly into the emitter electrode can be at least  $1 \times 10^{20} \text{ cm}^{-3}$ , which cannot be attained by the prior art, and thereby the interconnection resistance of the emitter electrode can be reduced.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross section showing a structure of a semiconductor device of a first embodiment of the invention;

Figs. 2 to 16 are schematic cross sections showing a process of manufacturing the semiconductor device of the first embodiment of the invention in accordance with the order of process steps;

Fig. 17 is a schematic cross section showing a structure in which an emitter electrode and an interconnection layer have a polycide structure in the first embodiment of the invention;

Fig. 18 is an equivalent circuit diagram showing a partial structure within a memory cell array of an SRAM;

Fig. 19 shows a structure of a memory cell in the SRAM;

Fig. 20 shows a relationship between a phosphorus concentration and a sheet resistance in the case where an emitter electrode and an interconnection layer are each formed of a single polycrystalline silicon film layer of 2000 Å in thickness doped with phosphorus;

Fig. 21 is an enlarged schematic cross section of a bipolar transistor region shown in Fig. 1 for showing reduction of a collector-emitter breakdown voltage;

Fig. 22 shows a relationship between a phosphorus concentration and a collector-emitter breakdown voltage  $BV_{CE0}$  in the case where an

emitter electrode and an interconnection layer are each formed of a single polycrystalline silicon film layer doped with phosphorus;

Fig. 23 shows a relationship between a phosphorus concentration and a sheet resistance in the case where an emitter electrode and an interconnection layer each have a polycide structure;

Fig. 24 shows a relationship between a phosphorus concentration and a direct contact resistance in the case where an emitter electrode and an interconnection layer have a polycide structure;

Fig. 25 shows a relationship between a phosphorus concentration and a collector-emitter breakdown voltage in the case where an emitter electrode and an interconnection layer have a polycide structure;

Fig. 26 is a schematic cross section showing a structure of a semiconductor device of a second embodiment of the invention;

Figs. 27 to 34 are schematic cross sections showing a process of manufacturing the semiconductor device of the second embodiment of the invention in accordance with the order of process steps;

Fig. 35 is a schematic cross section showing a structure in which an emitter electrode and an interconnection layer have a polycide structure in the second embodiment of the invention;

Figs. 36 and 37 show a process of forming an  $n^+$  emitter region in the first embodiment of the invention in accordance with the order of process steps;

Figs. 38 and 39 show a process of forming an  $n^+$  emitter region in the second embodiment of the invention in accordance with the order of process steps;

Figs. 40 to 42 show a process of forming an aperture in a self-aligned manner in the second embodiment of the invention in accordance with the order of process steps;

Fig. 43 is a schematic cross section showing a structure of a semiconductor device of a third embodiment of the invention;

Figs. 44 to 58 are schematic cross section showing a process of manufacturing the semiconductor device of the third embodiment of the invention in accordance with the order of process steps;

Fig. 59 is a schematic cross section showing a structure in which an emitter electrode and an interconnection layer have a polycide structure in the third embodiment of the invention;

Fig. 60 is a schematic cross section showing a manner in which an emitter aperture is formed in an insulating film on a base electrode by photolithography without providing a side wall



oxide film;

Fig. 61 is a schematic cross section showing a manner in which a side wall oxide film is formed in the third embodiment of the invention;

Fig. 62 is a schematic cross section showing a structure of a conventional semiconductor device;

Figs. 63 to 82 are schematic cross sections showing a process of manufacturing the conventional semiconductor device in accordance with the order of process steps;

Fig. 83 is an enlarged fragmentary cross section showing a region  $S_1$  in Fig. 79 for explaining the fact that a non-implanted region is generated;

Fig. 84 is an enlarged fragmentary cross section showing a region  $S_1$  in Fig. 79 for explaining the fact that the non-implanted region is generated;

Fig. 85 schematically shows resistances of various portions generated due to a polycrystalline silicon film doped with phosphorus;

Fig. 86 is a schematic cross section explaining a problem caused by RTA;

Fig. 87 shows a relationship between an annealing temperature and a carrier concentration in the case where arsenic and phosphorus are individually introduced into polycrystalline silicon at a concentration of  $2 \times 10^{19} \text{ cm}^{-3}$ ;

Fig. 88 shows a relationship between an impurity concentration and a resistivity in the case where arsenic and phosphorus are individually introduced into polycrystalline silicon; and

Fig. 89 is a fragmentary cross section explaining the fact that a base width of a base region decreases.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the invention will be described below with reference to the drawings.

### Embodiment 1

Referring to Fig. 1, a Bi-CMOS structure has a bipolar transistor region 10, an nMOS transistor region 20 and a pMOS transistor region 40, all of which are formed on a common semiconductor substrate.

In bipolar transistor region 10, an  $n^+$  buried layer 3 is formed on a surface of a  $p^-$  semiconductor substrate 1 made of silicon doped with impurity.  $p^-$  semiconductor substrate 1 is doped with p-type impurity at a concentration from  $1 \times 10^{15}$  to  $5 \times 10^{15} \text{ cm}^{-3}$ .  $n^+$  buried layer 3 is doped with n-type impurity at a concentration of about  $5 \times 10^{20} \text{ cm}^{-3}$ . On the surface of  $n^+$  buried layer 3, there are formed an  $n^-$  epitaxial growth layer 5 and an  $n^+$  diffusion layer 13 for leading a collector.  $n^-$  epitax-

ial growth layer 5 is doped with n-type impurity at a concentration of about  $1 \times 10^{16} \text{ cm}^{-3}$ .  $n^+$  diffusion layer 13 is doped with  $n^-$  type impurity at a concentration from about  $5 \times 10^{20}$  to about  $1 \times 10^{21} \text{ cm}^{-3}$ .

A  $p^-$  base region 7 and a  $p^+$  external base region 11 adjoining to each other are formed on the surface of  $n^-$  epitaxial growth layer 5.  $p^-$  base region 7 is doped with p-type impurity at a concentration of  $1 \times 10^{17}$  to  $1 \times 10^{18} \text{ cm}^{-3}$ .  $p^+$  external base region 11 is doped with p-type impurity at a concentration from  $5 \times 10^{20}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ . An  $n^+$  emitter region 9 is formed at a surface of  $p^-$  base region 7.  $n^+$  emitter region 9 is doped with n-type impurity at a concentration of  $5 \times 10^{20}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ .

A first interlayer insulating film 63 having a flattened top surface is formed over the surface of bipolar transistor region 10. First interlayer insulating film 63 is provided with an emitter aperture 63a reaching  $n^+$  emitter region 9. An emitter electrode 15 is formed on first interlayer insulating film 63 and is in contact with  $n^+$  emitter region 9 through emitter aperture 63a.

Emitter electrode 15 is made of polycrystalline silicon doped with phosphorus at a concentration in a range of from  $1 \times 10^{20} \text{ cm}^{-3}$  to  $6 \times 10^{20} \text{ cm}^{-3}$ .

Emitter electrode 15 is covered with a second interlayer insulating film 65 formed on first interlayer insulating film 63. Second interlayer insulating film 65 is provided with a contact hole 65a reaching emitter electrode 15. A conductive layer 71a is formed on second interlayer insulating film 65 and is in contact with emitter electrode 15 through contact hole 65a.

First and second interlayer insulating films 63 and 65 are provided with a contact hole 65b reaching  $p^+$  external base region 11 and a contact hole 65c reaching  $n^+$  diffusion layer 13. Conductive layers 71b and 71c are in contact with  $p^+$  external base region 11 and  $n^+$  diffusion layer 13 through contact holes 65b and 65c, respectively.

In nMOS transistor region 20, a  $p^-$  well region 23 is formed on the surface of  $p^-$  semiconductor substrate 1.  $p^-$  well region 23 is doped with p-type impurity at a concentration of about  $1 \times 10^{16} \text{ cm}^{-3}$ . nMOS transistors 30 are formed on the surface of  $p^-$  well region 23.

Each nMOS transistor 30 has a pair of n-type source/drain regions 25, a gate oxide film 27 and a gate electrode 29.

Each of paired n-type source/drain regions 25 has an LDD structure formed of two layers, i.e., a lightly doped  $n^-$  impurity region 25a and a heavily doped  $n^+$  impurity region 25b.  $n^-$  impurity region 25a is doped with n-type impurity at a concentration of about  $1 \times 10^{18} \text{ cm}^{-3}$ .  $n^+$  impurity region 25b is doped with n-type impurity at a concentration from  $5 \times 10^{20}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ . A gate electrode 29 is



formed on a region between paired source/drain regions 25 with a gate oxide film 27 therebetween.

An insulating film 31 made of a silicon oxide film is formed on the surface of each gate electrode 29. A side wall of gate electrode 29 is covered with a side wall oxide film 33.

nMOS transistor region 20 is covered with first interlayer insulating film 63 having a flattened top surface. First interlayer insulating film 63 is provided with an aperture 63b which reaches one of paired n-type source/drain regions 25. An interconnection layer 35 is formed on first interlayer insulating film 63 and is in contact with n-type source/drain regions 25 through aperture 63b.

Interconnection layer 35 is made of polycrystalline silicon doped with phosphorus at a concentration from  $1 \times 10^{20} \text{ cm}^{-3}$  to  $6 \times 10^{20} \text{ cm}^{-3}$ .

The surface of interconnection layer 35 is covered with a second interlayer insulating film 65 formed on the surface of first interlayer insulating film 63. Second interlayer insulating film 65 is provided with a contact hole 65d reaching a surface of a portion of interconnection layer 35. A conductive layer 71d is in contact with interconnection layer 35 through contact hole 65d.

First and second interlayer insulating films 63 and 65 are provided with a contact hole 65e reaching the other of paired n-type source/drain regions 25. A conductive layer 71e is in contact with n-type source/drain region 25 via contact hole 65e.

In pMOS transistor region 40, an  $n^+$  buried layer 41 is formed on the surface of  $p^-$  silicon substrate 1.  $n^+$  buried layer 41 is doped with n-type impurity at a concentration of about  $5 \times 10^{20} \text{ cm}^{-3}$ .  $n^-$  well region 43 is formed on the surface of  $n^+$  buried layer 41.  $n^-$  well region 43 is doped with n-type impurity at a concentration of about  $1 \times 10^{16} \text{ cm}^{-3}$ . A pMOS transistor 50 is formed on the surface of  $n^-$  well region 43.

pMOS transistor 50 has a pair of  $p^+$  source/drain regions 45, a gate oxide film 47 and a gate electrode 49.

Paired source/drain regions 45 are formed on the surface of  $n^-$  well region 43 and are spaced by a predetermined distance from each other.  $p^+$  source/drain regions 45 are doped with p-type impurity at a concentration from  $5 \times 10^{20}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ . A gate electrode 49 is formed on a region between paired source/drain regions 45 with a gate oxide film 47 therebetween.

An insulating film 51 made of a silicon oxide film is formed on the surface of gate electrode 49. A side wall of gate electrode 49 is covered with a side wall oxide film 53.

The surface of pMOS transistor region 40 is covered with first interlayer insulating film 63 having the flattened top surface. Second interlayer insulating film 65 is formed on the surface of first

interlayer insulating film 63. First and second interlayer insulating films 63 and 65 are provided with contact holes 65f reaching paired  $p^+$  source/drain regions 45. A conductive layer 71f is in contact with each of  $p^+$  source/drain regions 45 through contact hole 65f.

Element isolating oxide films 61 are provided for electrically isolating respective regions 10, 20 and 40, and others from each other.

A method of manufacturing the semiconductor device of the first embodiment of the invention will be described below.

Referring first to Fig. 2, the steps from the first step to that in Fig. 2 are the same as the steps in the conventional manufacturing process shown in Fig. 69, and thus, will not be described below.

Referring to Fig. 3, photoresist 91a is applied to the whole surface, and is exposed and developed. Thereby, a resist pattern 91a exposing the nMOS transistor region is formed. Using resist pattern 91a as a mask, impurity such as phosphorus is implanted at about 50keV and about  $2.0 \times 10^{13} \text{ cm}^{-2}$ . By this implantation,  $n^-$  impurity region 25a is formed at the surface of  $p^-$  well region 23. Thereafter, resist pattern 91a is removed.

Referring to Fig. 4, an LPCVD method is executed to form a silicon oxide film 33a of about 1500Å in thickness on the whole surface. Processing such as RIE is effected on silicon oxide film 33a.

Thereby, side wall oxide films 33 are formed to cover the side walls of gate electrodes 29, as shown in Fig. 5. By the above RIE, a thin silicon oxide film 27a at a lower level is simultaneously etched to form gate oxide films 27 and 47.

Referring to Fig. 6, photoresist 91b is applied to the whole surface, and is exposed and developed. Thereby, resist pattern 91b exposing the nMOS transistor region is formed. Using resist pattern 91b, gate electrodes 29 and side wall oxide films 33 as a mask, impurity such as arsenic is implanted into  $p^-$  well region 23 at about 50keV and  $4.0 \times 10^{15} \text{ cm}^{-2}$ . By this implantation  $n^+$  impurity regions 25b are formed.  $n^+$  impurity regions 25a and  $n^+$  impurity regions 25b form n-type source/drain regions 25 having the LDD structure. n-type source/drain regions 25, gate oxide film 27 and gate electrode 29 form nMOS transistor 30. Thereafter, resist pattern 91b is removed.

Referring to Fig. 7, photoresist 91c is applied to the whole surface, and is exposed and developed. Thereby, resist pattern 91c exposing predetermined portions of the pMOS transistor region and bipolar transistor region is formed. Using resist pattern 91c, gate electrode 49 and side wall oxide film 53 as a mask, impurity such as boron fluoride ( $\text{BF}_2$ ) is implanted at about 20keV and  $4.0 \times 10^{15} \text{ cm}^{-2}$ . By this implantation and others,

paired p' source/drain regions 45 are formed on the surface of n<sup>-</sup> well region 43 and also p' external base region 11 is formed on the surface of n<sup>+</sup> epitaxial growth layer 5. p<sup>+</sup> source/drain regions 45, gate oxide film 47 and gate electrode 49 form pMOS transistor 50. Thereafter, resist pattern 91c is removed. Then, heat treatment is executed, for example, at 850 °C for about 30 minutes, whereby implanted impurity is activated.

Referring to Fig. 8, photoresist 91d is applied to the whole surface, and is exposed and developed. Thereby, resist pattern 91d exposing a predetermined portion of bipolar transistor region 1a is formed. Using resist pattern 91d as a mask, impurity such as boron fluoride is implanted at about 50keV and  $1.0 \times 10^{14} \text{ cm}^{-2}$ . Owing to this implantation and others, p<sup>-</sup> base region 7 adjoining to p<sup>+</sup> external base region 11 is formed at the surface of n<sup>+</sup> epitaxial growth layer 5. Thereafter, resist pattern 91d is removed.

Referring to Fig. 9, a silicon oxide film 63a<sub>0</sub> having a thickness from about 6000Å to about 12000Å is formed on the whole surface by the LPCVD method. A film such as an SOG (Spin On Glass) film 67 is applied to the whole surface of silicon oxide film 63a<sub>0</sub>. When applying SOG film 67, SOG film 67 is in the form of liquid, so that the liquid is likely to be collected at concavities in stepped portions of the base, if any. Therefore, SOG film 67 thus formed has thick portions above the concavities. Thus, SOG film 67 has a substantially flat top surface. Thereafter, SOG film 67 and silicon oxide film 63a<sub>0</sub> are etched up to a level indicated by alternate long and short dash line by the RIE method. This etching is carried out under the conditions that etching rates of SOG film 67 and silicon oxide film 63a<sub>0</sub> are equal to each other.

Referring to Fig. 10, the above etching forms first interlayer insulating film 63 which has a thickness A<sub>1</sub> from about 500Å to about 3000Å at a position above the gate part and has a substantially flat top surface.

Referring to Fig. 11, a resist pattern 91e having a predetermined patterned configuration is formed on the surface of first interlayer insulating film 63b. Using this resist pattern 91e as a mask, processing such as RIE is effected. Thereby, emitter aperture 63a, which partially exposes the surface of p<sup>-</sup> base region 7, and aperture 63b, which partially exposes the surface of n<sup>-</sup> type source/drain region 25, are formed in first interlayer insulating film 63.

Referring to Fig. 12, arsenic is implanted, for example, at about 60keV and  $1.0 \times 10^{15} \text{ cm}^{-2}$  before removing resist pattern 91e. By this implantation, n<sup>+</sup> emitter region 9 is formed at the surface portion of p-base region 7 at the bottom of emitter aperture 63a. Thereafter, resist pattern 91e is removed.

Referring to Fig. 13, LPCVD is executed at a temperature of 590 °C under a pressure from 0.3 to 0.5 Torr with gas of silane (SiH<sub>4</sub>) and phosphine (PH<sub>3</sub>). Thus a polycrystalline silicon film 15b which contains phosphorus introduced into its whole surface and has a thickness from about 1000 to about 3000Å is formed. The concentration of phosphorus in polycrystalline silicon film 15b is in a range from about  $1.0 \times 10^{20}$  to about  $6.0 \times 10^{20} \text{ cm}^{-3}$ . Thereafter, polycrystalline silicon film 15b doped with phosphorus is patterned into a predetermined configuration by photolithography and etching.

Referring to Fig. 14, by this patterning, emitter electrode 15 is formed which is in contact with n<sup>+</sup> emitter region 9 through emitter aperture 63a, and interconnection layer 35 is formed which is in contact with n-type source/drain region 25 through aperture 63b.

Referring to Fig. 15, second interlayer insulating film 65 is formed on first interlayer insulating film 63 to cover emitter electrode 15 and interconnection layer 35. A resist pattern 91f having a predetermined patterned configuration is formed on the surface of second interlayer insulating film 65. Using resist pattern 91f as a mask, anisotropic etching is effected on first and second interlayer insulating films 63 and 65. Thereby, contact holes 65a, 65b, 65c, 65d, 65e and 65f each reaching the conductive layer or conductive region are formed. Thereafter, resist pattern 91f is removed.

Referring to Fig. 16, conductive layers 71a, 71b, 71c, 71d, 71e and 71f are formed to be in contact with conductive regions and others at the lower level through contact holes 65a, 65b, 65c, 65d, 65e and 65f, respectively.

In this embodiment, as shown in Fig. 1, emitter electrode 15 and interconnection layer 35 are each made of a single layer of polycrystalline silicon doped with phosphorus. Emitter electrode 15 and interconnection layer 35 according to the invention may have other structures such as a polycide structure as shown in Fig. 17.

Referring to Fig. 17, emitter electrode 15a is formed of polycrystalline silicon film 15b doped with phosphorus and a silicide layer 15c formed thereon. Interconnection layer 35a is formed of polycrystalline silicon film 35b doped with phosphorus and a silicide layer 35c formed on the surface thereof. Polycrystalline silicon films 15b and 35b are doped with phosphorus at a concentration from  $1 \times 10^{20} \text{ cm}^{-3}$  to  $1 \times 10^{21} \text{ cm}^{-3}$ .

More specifically, silicide layers 15c and 35c are made of material such as WSi<sub>2</sub> (tungsten silicide) or TiSi<sub>2</sub> (titanium silicide).

Structures other than those described above are the same as those shown in Fig. 1, and thus will not be described below.

In this embodiment, emitter electrode 15 and interconnection layer 35 shown in Fig. 1 are obtained by patterning polycrystalline silicon film 15b doped with phosphorus. Polycrystalline silicon film 15b is formed by the LPCVD method in such a manner that phosphorus is introduced thereinto during formation of the film. Phosphorus is diffused uniformly and entirely into polycrystalline silicon film 15b formed in this manner. Therefore, uniform diffusion of impurity into polycrystalline silicon can be achieved without requiring heat treatment at a high temperature by RTA.

Since the high temperature heat treatment by RTA can be eliminated, it is possible to prevent spreading of  $n^+$  impurity region 25b forming the LDD structure particularly in nMOS transistor 30. Therefore, disadvantages in the nMOS transistor 30 such as punch through and deterioration of characteristics relating to the resistance against hot electrons can be prevented. Therefore, it is possible to reduce various sizes such as a gate length of nMOS transistor 30, and thus the degree of integration can be improved easily.

Since the heat treatment by RTA can be eliminated, it is possible to prevent diffusion of impurity from emitter electrode 15 into  $p^-$  base region 7, which may be caused by the heat treatment by RTA. Therefore, such a disadvantage can be prevented that  $n^+$  emitter region 9 is formed deep in  $p^-$  base region 7 due to the diffusion and thereby a width of  $p^-$  base region 7 is reduced. Accordingly, even if the concentration of phosphorus in emitter electrode 15 is increased, the collector-emitter breakdown voltage is not deteriorated, and thus a good breakdown voltage characteristic can be maintained. It is possible to increase the concentration of phosphorus in the emitter electrode 15, and therefore, the interconnection resistance of emitter electrode 15 can be reduced while maintaining a good breakdown voltage characteristic.

As stated above, the concentration of phosphorus contained in emitter electrode 15 and interconnection layer 35 shown in Fig. 1 can be increased according to the semiconductor device formed by the manufacturing method of this embodiment. Therefore, it is possible to increase the concentration of phosphorus contained in emitter electrode 15 and interconnection layer 35 to at least  $1 \times 10^{20} \text{ cm}^{-3}$ , which cannot be achieved in the prior art.

Since the concentration of phosphorus in the polycrystalline silicon forming emitter electrode 15 and interconnection layer 35 can be  $1 \times 10^{20} \text{ cm}^{-3}$  or more, remarkable effects can be obtained, for example, in the following case.

Description will be made on the case where nMOS transistor 30 shown in Fig. 1 is used as a driver transistor of an SRAM (Static Random Access

Memory), and interconnection layer 35 is used as a ground line connected to a memory cell in the SRAM.

Referring to Figs. 18 and 19, when a word line WL is activated (i.e., selected to become high), access transistors A1 and A2 are turned on. Source/drains of access transistor A1 are connected to "L" of a storage node and, via a bit line load, to  $V_{cc}$  (High), respectively. Since a potential difference between "L" of the storage node and  $V_{cc}$  is large, a so-called column current flows in a direction indicated by an arrow in the figure.

Access transistor A2 is also turned on. However, its source/drains are connected to "H" of the storage node and  $V_{cc}$  (High), respectively, and a potential difference therebetween is small. Therefore, a column current hardly flows through access transistor A2.

As described above, column current I flows through the path of  $V_{cc} \rightarrow$  bit line load  $\rightarrow$  bit line  $\rightarrow$  access transistor A1 of memory cell  $\rightarrow$  storage node "L"  $\rightarrow$  driver transistor D1 of memory cell  $\rightarrow$  N1  $\rightarrow$  N0  $\rightarrow$  GND.

When column current I flows through the above path, the potential at "L" of the storage node rises if there is an interconnection resistance between N0 and N1. Thus, the potential of storage node rises to a value which is higher than the GND potential by a product of column current I and interconnection resistance between N0 and N1. As the potential of storage node rises, the level at "L" of the storage node approaches to "H".

The memory cell in the SRAM stores data by setting one of the storage nodes to "L" and setting the other storage node to "H". If one of the storage nodes rises from "L" toward "H", both of the storage nodes may be determined as "H". In this case, stored data is broken. Therefore, the rise of "L" potential of the storage node must be suppressed, and therefore, it is necessary to reduce the interconnection resistance between N0 and N1.

More specifically, if column current I is, for example, about  $200 \mu\text{A}$  and the potential at N1 is to be lower than about 0.20V, the resistance between N0 to N1 must be lower than  $1000 \Omega$ . Therefore, if the interconnection has a length of about  $10 \mu\text{m}$  and a width of about  $1 \mu\text{m}$  (10 sheets), it is necessary to employ a sheet resistance not more than about  $100 \Omega/\square$ .

Fig. 20 is a graph showing relation between phosphorus concentration and sheet resistance when phosphorus is introduced to a polycrystalline silicon film having the thickness of  $2000 \text{ \AA}$ . As can be seen from Fig. 20, the sheet resistance must be at most about  $100 \Omega/\square$ , so that the phosphorus concentration must be at least about  $1 \times 10^{20} \text{ cm}^{-3}$ .

Referring to Fig. 1 again, interconnection layer 35 connected to nMOS transistor 30 in this em-

bodiment has the phosphorus concentration not less than  $1 \times 10^{20} \text{cm}^{-3}$ . Therefore, even if nMOS transistor 30 is applied to the SRAM described above, breakage of data stored in the memory cell of the SRAM can be prevented.

In this embodiment, polycrystalline silicon forming emitter electrode 15 is doped with phosphorus at a concentration not more than  $6 \times 10^{20} \text{cm}^{-3}$ . Therefore, a good collector-emitter breakdown voltage  $BV_{CEO}$  can be ensured. The reason of this is as follows.

Collector-emitter breakdown voltage  $BV_{CEO}$  is one of important electrical parameters of the bipolar transistor. If breakdown voltage  $BV_{CEO}$  were lower than a voltage applied across the collector and emitter, it would not operate as a bipolar transistor.

Referring to Fig. 21, collector-emitter breakdown voltage  $BV_{CEO}$  depends on a pn junction breakdown voltage across collector 5 and base 7 if base width  $W_1$  is wide. However, if base width  $W_1$  is narrow, collector-emitter breakdown voltage  $BV_{CEO}$  depends on a punch through breakdown voltage across collector 5 and emitter 9. Punch through breakdown voltage across the collector and emitter is a voltage at the time when a large current flows due to the fact that a depletion layer between collector 5 and base 7 continues to a depletion layer between emitter 9 and base 5, and thereby a collector electric field reduces a diffusion potential between emitter 5 and base 7.

Referring to Fig. 22, if the phosphorus concentration is not more than  $6 \times 10^{20} \text{cm}^{-3}$ , a relatively small amount of phosphorus is diffused from the emitter electrode to the substrate. Therefore, collector-emitter breakdown voltage  $BV_{CEO}$  is maintained at about 7V. If the phosphorus concentration exceeds  $6 \times 10^{20} \text{cm}^{-3}$ , a relatively large amount of phosphorus is diffused from the emitter electrode to the substrate. Thereby, the emitter region is formed deep, and thus the base width decreases. Therefore, collector-emitter breakdown voltage  $BV_{CEO}$  decreases to a value not more than 7V. Accordingly, the concentration of phosphorus in the polycrystalline silicon must be at most  $6 \times 10^{20} \text{cm}^{-3}$ .

A reference value of collector-emitter breakdown voltage  $BV_{CEO}$  is 7V. This is determined taking into account the fact that a power supply voltage currently used in semiconductor devices is generally 5V. Thus, the breakdown voltage not less than 5V is required, and the reference value is set to 7V leaving a margin.

Description will be made on the case where emitter electrode 15a and interconnection layer 35a are made of a polycide structure as shown in Fig. 17.

Emitter electrode 15a and interconnection layer 35a including the polycide structure shown in Fig.

17 can be formed also by the manufacturing method of the embodiment. Therefore, polycrystalline silicon films 15b and 35b can be doped with phosphorus at a concentration not less than  $1 \times 10^{20} \text{cm}^{-3}$ . Thereby, the structure shown in Fig. 17 can achieve a remarkable effect that destruction of data stored in the SRAM can be prevented, similarly to the structure shown in Fig. 1.

However, if metal silicide is used as the silicide forming the polycide structure, the metal silicide layer has a low resistance. Therefore, a relationship shown in Fig. 23 exists between the concentration of phosphorus in the polycrystalline silicon forming the polycide structure and the sheet resistance of the polycide structure.

Fig. 23 shows a case where the polycide structure is formed of polycrystalline silicon having a film thickness of  $1000 \text{\AA}$  and  $\text{WSi}_2$  having a film thickness of  $1000 \text{\AA}$ .

Referring to Fig. 23, the sheet resistance of polycide is not more than  $30 \Omega/\square$  regardless of the concentration of phosphorus, and thus is lower than the above value of about  $1000 \Omega/\square$ . Therefore, the concentration of phosphorus in polycrystalline silicon forming the polycide structure can be substantially negligible from only the viewpoint of the interconnection resistance of the polycide structure.

However, the polycide structure generally has such a nature that metal silicide tends to absorb dopant in the polycrystalline silicon. Therefore, there is a remarkably high resistance at a direct contact portion to N1 in Figs. 18 and 19, i.e., at contact portion between emitter electrode 35a and n-type source/drain region 25 in Fig. 11. More specifically, the direct contact resistance remarkably increases above  $1000 \Omega$  if the concentration of phosphorus lowers below  $1 \times 10^{19} \text{cm}^{-3}$ .

In the example stated with reference to Figs. 18 and 19, the resistance between N0 and N1 must be at less about  $1000 \Omega$ . However, if the polycide structure is employed, and the concentration of phosphorus is not more than  $1 \times 10^{19} \text{cm}^{-3}$ , even the direct contact resistance itself exceeds  $1000 \Omega$ .

In order to reduce the direct contact resistance to  $1000 \Omega$  or less, the concentration of phosphorus in the polycrystalline silicon must be  $1 \times 10^{19} \text{cm}^{-3}$  or more. It is necessary to take not only the direct contact resistance but also the interconnection resistance of polycide into consideration. Taking them into consideration, the concentration of phosphorus in the polycrystalline silicon forming the polycide structure must be  $1 \times 10^{20} \text{cm}^{-3}$  or more in order to prevent destruction of data stored in a memory cell in the SRAM.

In connection with this, the concentration of phosphorus in the polycrystalline silicon forming the polycide structure is not smaller than  $1 \times 10^{20} \text{cm}^{-3}$  in the embodiment. Therefore, the

structure shown in Fig. 17 has a remarkable advantage that destruction of data stored in the memory cell of the SRAM can be prevented.

In the case where emitter electrode 15a and interconnection layer 35a use the polycide structure as shown in Fig. 17, the upper limit of concentration of phosphorus in the polycrystalline silicon forming polycide is  $1 \times 10^{21} \text{cm}^{-3}$ .

The reason is substantially the same as that relating to the upper limit already described with reference to Fig. 1. However, the polycide structure has the nature that the metal silicide tends to absorb dopant in the polycrystalline silicon as state before. Therefore, the amount of phosphorus diffused into the substrate from the emitter electrode having the polycide structure is smaller than that in the structure shown in Fig. 1 by the amount of absorbed dopant.

Therefore, collector-emitter breakdown voltage  $BV_{CEO}$  does not lower below 7V unless the concentration of phosphorus in the polycrystalline silicon forming the polycide structure as shown in Fig. 25 exceeds  $1 \times 10^{21} \text{cm}^{-3}$ . Therefore, phosphorus can be introduced into the polycrystalline silicon at the concentration up to  $1 \times 10^{21} \text{cm}^{-3}$ .

By the reasons described above, the upper limit of concentration of phosphorus in the polycrystalline silicon forming the polycide structure is not more than  $1 \times 10^{21} \text{cm}^{-3}$ .

## Embodiment 2

Referring to Fig. 26, a semiconductor device of a second embodiment includes a silicon oxide film 101 and a silicon nitride film 103 in addition to the structure of the first embodiment.

Silicon oxide film 101 has a thickness of about  $300 \text{\AA}$  and is formed at the whole surface of substrate provided with the bipolar transistor, nMOS transistor 30 and pMOS transistor 50. Silicon nitride film 103 is formed on the whole surface of silicon oxide film 101 and has a thickness from about  $500$  to about  $1000 \text{\AA}$ . Structures other than the above are substantially the same as those of the semiconductor device of the first embodiment, and thus will not be described.

A method of manufacturing the semiconductor device of the second embodiment will be described below.

According to the manufacturing method of this embodiment, the same steps as those of the first embodiment shown in Figs. 2 to 8 are first executed. Then, silicon oxide film 101 of about  $300 \text{\AA}$  in thickness and silicon nitride film 103 from about  $500$  to about  $1000 \text{\AA}$  in thickness are sequentially deposited on the whole surface by the LPCVD method. A silicon oxide film 63a<sub>0</sub> from about  $6000$  to about  $12000 \text{\AA}$  in thickness is formed on the

whole surface of silicon nitride film 103 by the LPCVD method. A film such as SOG film 67 is applied to the whole surface of silicon oxide film 63a<sub>0</sub>, and its top surface is substantially flattened to form the structure shown in Fig. 27.

Referring to Fig. 27, etching, for example, by the RIE method is effected on SOG film 67 and silicon oxide film 63a<sub>0</sub> under the conditions that etching rates of SOG film 67 and silicon oxide film 63a<sub>0</sub> are equal to each other.

Referring to Fig. 28, by this etching first interlayer insulating film 63 is formed which has a thickness from about  $500 \text{\AA}$  to about  $3000 \text{\AA}$ , at a position above the gate part and has the substantially flat top surface.

Referring to Fig. 29, photoresist 91e is applied to the whole surface of first interlayer insulating film 63, and is exposed and developed. Thereby, resist pattern 91e having a predetermined patterned configuration is formed. Using this resist pattern 91e as a mask, first interlayer insulating film 63 is etched by RIE. This etching is carried out under the conditions that an etch selectivity, for example, with respect to silicon nitride film 103 is high. By this etching, apertures reaching the surface of silicon nitride film 103 are formed at predetermined regions. Then, silicon nitride film 103 exposed at bottoms of the apertures are etched by RIE under the conditions that the etch selectivity with respect to the silicon oxide film is high. Thereafter, portions of silicon oxide film 101 exposed at the bottoms of apertures 163b<sub>1</sub> and 163a<sub>1</sub> are etched by RIE to expose the surface of substrate under the conditions that the etch selectivity with respect to silicon is high.

Referring to Fig. 30, by the above etching, an emitter aperture 163a exposing the surface of n<sup>+</sup> emitter region 9 and an aperture 163b partially exposing the surface of n-type source/drain region 25 are formed. Thereafter, impurity such as arsenic is implanted at about  $60 \text{keV}$  and  $1.0 \times 10^{15} \text{cm}^{-2}$ . By this implantation and others, n<sup>+</sup> emitter region 9 is formed within p<sup>-</sup> base region 7. Thereafter, resist pattern 91e is removed.

Referring to Fig. 31, LPCVD is executed at a temperature of  $590^\circ \text{C}$  under a pressure from  $0.3$  to  $0.5$  Torr with gas of silane and phosphine. Thereby, a polycrystalline silicon film 15b is doped with phosphorus is formed on the whole surface. Polycrystalline silicon film 15b is substantially uniformly doped with phosphorus at a concentration from  $1.0 \times 10^{20} \text{cm}^{-3}$  to  $6.0 \times 10^{20} \text{cm}^{-3}$ . Thereafter, polycrystalline silicon film 15b is patterned into a predetermined configuration.

Referring to Fig. 32, by this patterning, emitter electrode 15 being in contact with the n<sup>+</sup> emitter region through emitter aperture 163a and interconnection layer 35 being in contact with n-type

source/drain region 25 through aperture 163b are formed.

Referring to Fig. 33, second interlayer insulating film 65 covering emitter electrode 15 and interconnection layer 35 is formed on the whole surface of first interlayer insulating film 63. Resist pattern 91f having a predetermined patterned configuration is formed on the surface of second interlayer insulating film 65. Using this resist pattern 91f as a mask, etching is successively effected on first and second interlayer insulating films 63 and 65. By this etching, contact holes 65a, 65b, 65c, 65d, 65e and 65f are formed which reach the conductive layers or conductive regions at the lower level. Thereafter, resist pattern 91f is removed.

Referring to Fig. 34, contact holes 71a, 71b, 71c, 71d, 71e and 71f are formed, which are in contact with the conductive layers or conductive regions at the lower level through contact holes 65a, 65b, 65c, 65d, 65e and 65f, respectively.

The second embodiment has been described in connection with the case where each of emitter electrode 15 and interconnection layer 35 is formed of a single polycrystalline silicon film layer doped with phosphorus. This embodiment, however, is not restricted thereto, and it may employ emitter electrode 15 and interconnection layer 35 having a polycide structure as shown in Fig. 35.

Referring to Fig. 35, an emitter electrode 15a and an interconnection layer 35a have a polycide structure. Specifically, emitter electrode 15a and interconnection layer 35a each have a polycrystalline silicon film 15b or 35b doped with phosphorus and a silicide layer 15c or 35c formed thereon.

Polycrystalline silicon films 15b and 35b are doped with phosphorus at a concentration of  $1.0 \times 10^{20} \text{cm}^{-3}$  from  $1.0 \times 10^{21} \text{cm}^{-3}$ . Silicide layers 15c and 35c are made of, for example,  $\text{TiSi}_2$  (titanium silicide),  $\text{WSi}_2$  (tungsten silicide) or  $\text{CoSi}_2$  (cobalt silicide).

According to the manufacturing method of this embodiment, a polycrystalline silicon film forming emitter electrode 15 shown in Fig. 26 is formed to contain phosphorus by the LPCVD method, which is similar to the first embodiment. Therefore, heat treatment at a high temperature by RTA is not required, and thus the degree of integration can be improved easily.

Since the heat treatment by RTA can be eliminated, the concentration of phosphorus in the polycrystalline silicon forming emitter electrode 15 can be increased, so that the interconnection resistance can be reduced.

Therefore, the Bi-CMOS structure manufactured by the manufacturing method of this embodiment can increase the concentration of phosphorus in the polycrystalline silicon, which forms emitter electrode 15 and interconnection layer 35, to a

value not less than  $1 \times 10^{20} \text{cm}^{-3}$ . Therefore, this embodiment can achieve a remarkable effect, for example, that destruction of data stored in a memory cell in the SRAM can be prevented similarly to the first embodiment.

According to the Bi-CMOS structure of this embodiment, if each of emitter electrode 15 and interconnection layer 35 is formed of a single polycrystalline silicon layer (see Fig. 26), the concentration of phosphorus in the polycrystalline silicon film is not more than  $6 \times 10^{20} \text{cm}^{-3}$ . If emitter electrode 15a and interconnection layer 35a have the polycide structure (see Fig. 35), the concentration of phosphorus in the polycrystalline silicon film forming the polycide structure is not more than  $1 \times 10^{21} \text{cm}^{-3}$ . Therefore, a good collector-emitter breakdown voltage can be obtained similarly to the first embodiment.

This embodiment is additionally provided with silicon oxide film 101 and silicon nitride film 103. Owing to this, (i) a good collector-emitter breakdown voltage can be maintained, and (ii) the degree of integration can be improved easily. The reason will be described below.

(i) Maintenance of the collector-emitter breakdown voltage

Referring first to Fig. 36, etching is effected on first interlayer insulating film 63 with a mask so as to form aperture 163a. Since a film thickness  $T_{21}$  of first interlayer insulating film 63 is not initially uniform, first interlayer insulating film 63 is generally over-etched to an extent of about 10% of its film thickness. This over-etches the surface of  $p^-$  base region 7, so that a deep groove having a thickness  $T_{22}$  is formed at the surface of  $p^-$  base region 7.

Referring to Fig. 37,  $n^+$  emitter region 9 is formed in the structure provided with the groove. Formation of  $n^+$  emitter region 9 is effected, for example, by ion implantation with a predetermined implantation energy. Therefore,  $n^+$  emitter region 9 is formed deeper by the depth  $T_{22}$  of the groove, and thereby a base width  $W_{20}$  of  $p^-$  base region 7 is reduced. Accordingly, the first embodiment may not ensure a good collector-emitter breakdown voltage.

Referring to Fig. 38, the second embodiment is provided with silicon oxide film 101 and silicon nitride film 103. Silicon nitride film 103 serves as an etch stopper when etching first interlayer insulating film 63. Silicon oxide film 101 serves as an etch stopper in etching silicon nitride film 103.

Opening 163a is extended to the surface of  $p^-$  base region 7 by the etching of silicon oxide film 101. Silicon oxide film 101 has a film thickness  $T_{11}$ , which is set to be remarkably smaller than film

thickness  $T_{21}$  of first interlayer insulating film 63 shown in Fig. 36.

More specifically, film thickness  $T_{11}$  of silicon oxide film 101 is 300Å while film thickness  $T_{21}$  of first interlayer insulating film 63 is from 4500 to 7000Å. Therefore, even if over-etching of 10% is effected on the silicon oxide film 101, a depth  $T_{12}$  of the groove formed at the surface of  $p^-$  base region 7 is much smaller than depth  $T_{22}$  of the groove formed in the first embodiment.

Accordingly,  $n^+$  emitter region 9 is not formed at so deep a position as shown in Fig. 39, and an intended base width  $W_{10}$  can be obtained. Therefore, a good collector-emitter breakdown voltage can be maintained.

#### (ii) Improvement of degree of integration

Since this embodiment is provided with silicon oxide film 101 and silicon nitride film 103, it is possible to form, e.g., an aperture 163b shown in Fig. 26 in a self-aligned manner.

Referring to Fig. 40, a first opening 163c<sub>1</sub> is formed at first interlayer insulating film 63 using photolithography and etching. During this etching, silicon nitride film 103 serves as an etching stopper. Thereafter, wet etching is successively effected on silicon nitride film 103 and silicon oxide film 101.

Referring to Fig. 41, by this wet etching, aperture 163c<sub>2</sub> is formed exposing the surface of  $n^-$  type source/drain region 25.

Referring to Fig. 42, interconnection layer 35e is formed to be in contact with the exposed surface of  $n^-$  type source/drain region 25 through the aperture 163c.

If aperture 163c is formed in the self-aligned manner as described above, a distance  $L_{p2}$  between the gate electrode 29 and interconnection layer 35e can be made shorter than a distance of possible misalignment of the mask.

Meanwhile, as to aperture 163b shown in Fig. 26, a side surface of gate electrode 29 may be exposed at a side wall of aperture 163b due to misalignment of the mask at the process shown in Figs. 29 and 30. In this case, gate electrode 29 and polycrystalline silicon film 15b are short-circuited when polycrystalline silicon 15b is formed at the process in Fig. 31.

In order to prevent the short-circuit, distance  $L_{p1}$  between gate electrode 29 and interconnection layer 35 shown in Fig. 26 must be larger than a distance (from about 0.1 to about 0.2μm) of possible misalignment of the mask. Meanwhile, an inner diameter  $L_{c1}$  of aperture 63b cannot be reduced below a predetermined size (about 0.4 to about 0.5μm) due to limitation by photolithography. Therefore, as distance  $L_{p1}$  between gate electrode

29 and interconnection layer 35 increases, a distance  $L_{w1}$  between gate electrodes 29 inevitably increases. Consequently, it is difficult to attain the high integration with the aperture 63b shown in Fig. 26.

Meanwhile, according to the self-aligned manner described before, a mask is not required when etching the silicon nitride film and silicon oxide film 101. Therefore, it is not necessary to take into account the misalignment of the mask. Therefore, as shown in Fig. 42, a distance  $L_{p2}$  between gate electrode 29 and interconnection layer 35e can be made smaller than the distance of possible misalignment of the mask. Accordingly, a distance  $L_{w2}$  between gate electrodes 29 can be reduced in accordance with reduction of distance  $L_{p2}$ , and thus high integration can be achieved.

#### Embodiment 3

Referring to Fig. 43, a Bi-CMOS structure has a bipolar transistor region 210, an nMOS transistor region 220 and pMOS transistor region 240 all of which are formed on the same semiconductor substrate.

The Bi-CMOS structure in this embodiment differs from the second embodiment in the structure of bipolar transistor region 210.

In bipolar transistor region 210,  $n^+$  buried layer 3 is formed on the surface of  $p^-$  semiconductor substrate 1 made of silicon doped with impurity.  $n^-$  epitaxial growth layer 5 and  $n^+$  diffusion layer 13 for leading the collector are formed on the surface of  $n^+$  buried layer 3.

A  $p^-$  base region 207 and a  $p^+$  external base region 211 adjoining to each other are formed on the surface of  $n^-$  epitaxial growth layer 5. An  $n^+$  emitter region 209 is formed within  $p^-$  base region 207. Bipolar transistor region 210 is covered with first interlayer insulating film 63. First interlayer insulating film 63 is provided with an aperture 263d communicated with  $p^-$  base region 207,  $n^+$  emitter region 209 and  $p^+$  external base region 211.

A base leading electrode 217 is formed on the surface of first interlayer insulating film 63 and is in contact with  $p^+$  external base region 211 through aperture 263d. A silicon oxide film 218 is formed on base electrode 217. An end surface (i.e., side surface) of base leading electrode 217 is covered with a side wall oxide film 219. An emitter aperture 219a, which has a configuration defined by side wall oxide film 219 and reaches the surface of  $n^+$  emitter region 209, is formed in base aperture 263d.

An emitter electrode 215 is in contact with  $n^+$  emitter region 209 through emitter aperture 219a. Emitter electrode 215 is made of polycrystalline silicon which is doped with phosphorus at a con-



centration from  $1 \times 10^{20} \text{cm}^{-3}$  to  $6 \times 10^{20} \text{cm}^{-3}$ .

Emitter electrode 215 and base electrode 217 are covered with second interlayer insulating film 65 formed on the surface of first interlayer insulating film 63. Second interlayer insulating film 65 is provided with contact holes 65a and 65b reaching emitter electrode 215 and base electrode 217, respectively. Conductive layers 71a and 71b are in contact with emitter electrode 215 and base electrode 217 through contact holes 65a and 65b, respectively.

First and second interlayer insulating films 63 and 65 are also provided with a contact hole 65c reaching  $n^+$  diffusion layer 13. A conductive layer 71c is in contact with  $n^+$  diffusion layer 13 through contact hole 65c.

Structures other than those in bipolar transistor region 210 is substantially the same as those of the second embodiment, and thus will not be described below.

A method of manufacturing the semiconductor device of the third embodiment of the invention will be described below.

Referring to Fig. 44, a process from the first step to the step shown in Figure 44 is the same as that in the manufacturing method of the first embodiment shown in Fig. 6, and thus will not be described below.

Referring to Fig. 45, photoresist is applied to the whole surface, and is exposed and developed. Thereby, a resist pattern 291c exposing the pMOS transistor region is formed. Using resist pattern 291c as a mask, impurity such as  $\text{BF}_2$  is implanted at about 20keV and  $4.0 \times 10^{15} \text{cm}^{-2}$ . Thereby, a pair of  $p^+$  source/drain regions 45 are formed at the surface of  $n^-$  well region 43. A pair of source/drain regions 45, gate oxide film 47 and gate electrode 49 form pMOS transistor 50. Thereafter, resist pattern 291c is removed.

Referring to Fig. 46, silicon oxide film 101 of about 300Å in thickness and silicon nitride film 103 from about 500 to about 1000Å in thickness are formed on the whole surface by the LPCVD method. Silicon oxide film 63a<sub>0</sub> from about 6000 to about 12000Å in thickness is formed on the whole surface of silicon nitride film 103 by the LPCVD method. A film such as SOG film 67 is applied to the surface of silicon oxide film 63a. Since SOG film 67 is liquid, it tends to be collected in cavities at stepped portions on the base, if any. Therefore, SOG film 67 has thick portions above the cavities, and has a substantially flat top surface. Thereafter, SOG film 67 and silicon oxide film 63a are etched up to a level indicated by alternate long and short dash line, by e.g. the RIE method under the conditions that etching rates of SOG film 67 and silicon oxide film 63a are equal to each other.

Referring to Fig. 47, by the above etching, first interlayer insulating film 63 is formed which has a thickness  $A_3$  from about 500Å to about 3000Å at a position above the gate part and has a substantially flat top surface.

Referring to Fig. 48, photoresist is applied to the whole surface of first interlayer insulating film 63, and is exposed and developed. Thereby, a resist pattern 291g having a hole pattern located above a predetermined region of the bipolar transistor region is formed. Using this resist pattern 291g as a mask, first interlayer insulating film 63 is etched by the RIE method to expose the top surface of silicon nitride film 103. This etching is carried out under the conditions that the etching selection ratio, for example, with respect to silicon nitride film 103 is high. Then, silicon nitride film 103 is etched by RIE to expose the top surface of silicon oxide film 101 under the conditions that the etch selectivity with respect to silicon oxide film 101 is high. Further, silicon oxide film 101 is etched by RIE to expose the surface of  $n^+$  epitaxial growth layer 5 under the conditions that the etch selectivity with respect to silicon is high. Thus a base aperture 263d is formed partially exposing the surface of  $n^+$  epitaxial growth layer 5. Thereafter, resist pattern 291g is removed.

Referring to Fig. 49, a polycrystalline silicon film 217a of about 2000Å in thickness is formed on the whole surface by the LPCVD method. Impurity such as  $\text{BF}_2$  is implanted into the whole surface of polycrystalline silicon film 217a at about 40keV and about  $4.0 \times 10^{15} \text{cm}^{-2}$ . A silicon oxide film 218a of about 2000Å in thickness is formed by the LPCVD method on the whole surface of polycrystalline silicon film 217a.

Referring to Fig. 50, a resist pattern 291h having an intended configuration is formed on a predetermined region of silicon oxide film 218a. Using resist pattern 291h as a mask, etching is successively effected on silicon oxide film 218a and polycrystalline silicon film 217a. By this etching, a base electrode 217 is formed which is in contact with the surface of  $n^+$  epitaxial growth layer 5 through base aperture 263d. An emitter aperture results from the formation of base electrode 217. Thereafter, a predetermined heat treatment is effected, whereby boron in base electrode 217 is diffused into  $n^+$  epitaxial growth layer 5 and thereby  $p^+$  external base region 211 is formed.

Referring to Fig. 51, impurity such as  $\text{BF}_2$  is implanted at about 50keV and  $1.0 \times 10^{14} \text{cm}^{-2}$ . By this implantation and others,  $p^-$  base region 207 is formed which adjoins to  $p^+$  external base region 211, on the surface of  $n^+$  epitaxial growth layer 5. Thereafter, resist pattern 291h is removed.

Referring to Fig. 52, a silicon oxide film (not shown) of about 2000Å in thickness is formed on

the whole surface by the LPCVD method, and then the whole surface of this silicon oxide film is etched, for example, by RIE. By this etching, the side wall oxide film 219 covering the end surface (side surface) of base electrode 217 is formed. Also emitter aperture 219a is formed and defined by the surface of side wall oxide film 219.

Referring to Fig. 53, using side wall oxide film 219 as a mask, impurity such as arsenic is implanted at about 60keV and  $1.0 \times 10^{15} \text{cm}^{-2}$ . This implantation forms  $n^+$  emitter region 209 at the surface of  $p^-$  base region 207.

Referring to Fig. 54, photoresist is applied to the whole surface, and is exposed and developed. Thereby, a resist pattern 291e having an intended configuration is formed. Using resist pattern 291e as a mask, first interlayer insulating film 63, silicon nitride film 103 and silicon oxide film 101 are sequentially etched, for example, by RIE. This etching forms aperture 163b partially exposing the surface of  $n$ -type impurity region 25. Thereafter, resist pattern 291e is removed.

Referring to Fig. 55, LPCVD is executed at a temperature of  $590^\circ\text{C}$  under a pressure from 0.3 to 0.5 Torr with gas of silane and phosphine. Thus polycrystalline silicon film 15b doped with phosphorus and having a thickness of about  $2000\text{\AA}$  is formed. The concentration of phosphorus in polycrystalline silicon film 15b is in a range from about  $1.0 \times 10^{20} \text{cm}^{-3}$  to about  $6.0 \times 10^{20} \text{cm}^{-3}$ . Thereafter, polycrystalline silicon film 15b is patterned by photolithography and etching.

Referring to Fig. 56, by this patterning, emitter electrode 215, which is in contact with  $n^+$  emitter region 209 through emitter aperture 219a, and interconnection layer 35 which is in contact with  $n$ -type source/drain region 25 through aperture 163b are formed.

Referring to Fig. 57, second interlayer insulating film 65 is formed on the whole surface of first interlayer insulating film 63 to cover emitter electrode 215 and interconnection layer 35. A resist pattern 291f having a predetermined configuration is formed on second interlayer insulating film 65. Using resist pattern 291f as a mask, etching is effected on first and second interlayer insulating films 63 and 65, e.g., by RIE. Thereby, contact holes 65a, 65b, 65c, 65d, 65e and 65f are formed in the first and second interlayer insulating films. Thereafter, resist pattern 291f is removed.

Referring to Fig. 58, conductive layers 71a, 71b, 71c, 71d, 71e and 71f are formed to be in contact with conductive layers or conductive regions through contact holes 65a, 65b, 65c, 65d, 65e or 65f, respectively.

In this embodiment, emitter electrode 15 and interconnection layer 35 are each made of a single polycrystalline silicon film layer doped with phos-

phorus. Emitter electrode 15 and interconnection layer 35 may have different structure, and specifically may have a polycide structure as shown in Fig. 59.

Referring to Fig. 59, an emitter electrode 215a has the polycide structure, and is formed of a polycrystalline silicon film 215b and a metal silicide layer 215c formed thereon. Polycrystalline silicon film 215b is doped with phosphorus at a concentration from  $1 \times 10^{20} \text{cm}^{-3}$  to  $1 \times 10^{21} \text{cm}^{-3}$ .

Interconnection layer 35a also has a polycide structure and is formed of polycrystalline silicon film 35b and metal silicide layer 35c formed thereon. Polycrystalline silicon film 35b is doped with phosphorus at a concentration from  $1 \times 10^{20} \text{cm}^{-3}$  to  $1 \times 10^{21} \text{cm}^{-3}$ .

According to the manufacturing method of this embodiment, the polycrystalline silicon film which forms emitter electrode 215 and interconnection layer 35 and contains phosphorus is formed by the LPCVD method after  $n^+$  emitter region 209 is formed in  $p^-$  base region 207, similarly to the first embodiment. Therefore, heat treatment at a high temperature by RTA is not required, and thus the degree of integration can be improved easily. Since the heat treatment by RTA can be eliminated, the concentration of phosphorus in the polycrystalline silicon forming emitter electrode 215 and interconnection layer 35 can be increased, so that the interconnection resistance can be reduced.

Therefore, the Bi-CMOS structure manufactured by the manufacturing method of this embodiment can increase the concentration of phosphorus in the polycrystalline silicon forming emitter electrode 215 and interconnection layer 35 to at least  $1 \times 10^{20} \text{cm}^{-3}$ . Therefore, it can achieve a remarkable effect. For example, that destruction of data stored in a memory cell in the SRAM can be prevented, similarly to the first embodiment.

If each of emitter electrode 215 and interconnection layer 35 is formed of a single polycrystalline silicon film layer (see Fig. 43), the concentration of phosphorus in the polycrystalline silicon film is not more than  $6 \times 10^{20} \text{cm}^{-3}$ . If emitter electrode 215a and interconnection layer 35a have the polycide structure (see Fig. 59), the concentration of phosphorus in the polycrystalline silicon film forming the polycide structure is not more than  $1 \times 10^{21} \text{cm}^{-3}$ . Therefore, a good collector-emitter breakdown voltage can be obtained similarly to the first embodiment.

This embodiment is additionally provided with silicon oxide film 101 and silicon nitride film 103. Owing to this, a good collector-emitter breakdown voltage can be maintained, and the degree of integration can be improved easily, similarly to the second embodiment.

Since this embodiment is additionally provided with side wall oxide film 219a, the base resistance can be reduced and the degree of integration can be further improved.

Referring to Fig. 60, the process for forming emitter aperture 218b by photolithography must be executed, taking into account the possible misalignment of the mask. If the mask were misaligned, emitter aperture 218b would not be formed at a predetermined position and would be dislocated. If misaligned, the end surface (side surface) 217e of base electrode 217 might be exposed at the side wall of emitter aperture 218b. If the emitter electrode were formed while the end surface (side surface) 217e of base electrode 217 was exposed, base electrode 217 and the emitter electrode would be short-circuited.

In order to prevent this short-circuit, a distance  $L_{M2}$  between base electrode 27 and emitter aperture 218b must be larger than a distance of possible misalignment of the mask. The large distance  $L_{M2}$  increases a distance between  $p^+$  external base region 211 and  $n^+$  emitter region 209, resulting in a disadvantage that a large parasitic capacitance  $r_1$  is produced therebetween.

According to this embodiment, however, the end surface (side surface) 217e of base electrode 217 is covered with side wall oxide film 219 as shown in Fig. 61. In forming side wall oxide film 219, a mask is not required as already stated in connection with the process shown in Fig. 52, so that it is not necessary to take into account the misalignment of the mask. Therefore, distance  $L_{M1}$  between base electrode 217 and emitter aperture 219a can be made smaller than the distance of possible misalignment of the overlapped mask.

Since  $n^+$  emitter region 209 is formed using side wall oxide film 219 as a mask, a distance between  $p^+$  external base region 211 and  $n^+$  emitter region 209 decreases as distance  $L_{M1}$  decreases. Therefore, a parasitic resistance (base resistance) generated between  $p^+$  external base region 211 and  $n^+$  emitter region 209 can be made small.

Since distance  $L_{M1}$  between  $p^+$  external base region 211 and  $n^+$  emitter region 209 can be reduced, the degree of integration can be improved corresponding to the reduction of distance.

The first, second and third embodiments have been described in connection with the cases where emitter electrodes 15 and 215 and interconnection layer 35 are each formed of the single polycrystalline silicon film layer doped with phosphorus and where they are formed of the polycide structures each including the single polycrystalline silicon film layer doped with phosphorus. However, other structures may be employed. Emitter electrode 215 and interconnection layer 15 are required only to in-

clude polycrystalline silicon films doped with phosphorus at a predetermined concentration.

In the first, second and third embodiments,  $n^+$  emitter regions 9 and 209 are formed by introducing impurity into  $p^-$  base region 7 by ion implantation. However, different process may be employed.  $n^+$  emitter regions 9 and 209 may be formed by any method provided that they are formed prior to formation of emitter electrodes 15 and 215.

Further, the first, second and third embodiments, which have been described in connection with the Bi-CMOS structure, are not restricted to this. The invention can be applied to any semiconductor device including bipolar transistors.

The method of manufacturing the semiconductor device of the invention can prevent disadvantages such as punch through and deterioration of characteristics relating to resistance against hot electrons in the MOS transistor. Therefore, sizes of various portions such as a gate length in the MOS transistor can be reduced, and thus the degree of integration can be improved easily.

Since heat treatment by RTA can be eliminated, a disadvantage caused by the heat treatment can be prevented, and specifically it is possible to prevent a disadvantage that the emitter impurity region is formed deep in the base impurity region, and thereby the width of base impurity region decreases. Accordingly, the interconnection resistance of emitter electrode can be reduced while maintaining a good breakdown voltage characteristic.

According to the semiconductor device of the invention manufactured by the method described above, the concentration of phosphorus in the polycrystalline silicon film can be large. Accordingly, the concentration of phosphorus in the emitter electrode can be increased to at least  $1 \times 10^{20} \text{ cm}^{-3}$ , which cannot be attained in the prior art, and thus the interconnection resistance of emitter electrode can be reduced.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

## Claims

1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a collector impurity region (3, 5, 13) of a first conductivity type at a main surface of a semiconductor substrate (1);

forming a base impurity region (7, 11; 207, 211) of a second conductivity type at the main

surface of said semiconductor substrate within said collector impurity region;

forming an emitter impurity region (9: 209) of the first conductivity type at the main surface of said semiconductor substrate within said base impurity region; and

forming a polycrystalline silicon layer (15: 15b: 215: 215b), which is uniformly doped with phosphorus and adjoins to said emitter impurity region, by a vapor deposition method.

2. The method of manufacturing the semiconductor device according to claim 1, wherein

said step of forming said emitter impurity region (9: 209) includes the step of ion-implanting impurity of the first conductivity type into said base impurity region (7, 11: 207, 211).

3. The method of manufacturing the semiconductor device according to claim 1 or 2, wherein

said vapor deposition method for forming said polycrystalline silicon layer (15: 15b: 215: 215b) is executed in an atmosphere containing phosphorus.

4. The method of manufacturing the semiconductor device according to claim 3, wherein

said vapor deposition method for forming said polycrystalline silicon layer (15: 15b: 215: 215b) is executed in an atmosphere containing silane ( $\text{SiH}_4$ ) and phosphine ( $\text{PH}_3$ ).

5. The method of manufacturing the semiconductor device according to one of claims 1 to 4, further comprising the step of forming a silicide layer (15c: 215c) on said polycrystalline silicon layer (15b: 215b) to be in contact with said polycrystalline silicon layer.

6. The method of manufacturing the semiconductor device according to one of claims 1 to 5, further comprising the steps of:

forming a first insulating layer (101) on the main surface of said semiconductor substrate (1);

forming on said first insulating layer a second insulating layer (103) having different etch characteristic than that of said first insulating layer;

forming on said second insulating layer a third insulating film layer (63) having different etch characteristic than said second insulating layer; and

etching said first, second and third insulating layers to form in said first, second and third insulating layers an aperture (163a<sub>2</sub>: 263d) reaching said emitter impurity region (9:

209); wherein

said polycrystalline silicon layer (15: 15b: 215: 215b) is formed to be in contact with said emitter impurity region through said aperture.

7. The method of manufacturing the semiconductor device according to claim 6, wherein

each of said first and third insulating layers (101, 63) includes a silicon oxide film, and said second insulating layer (103) includes a silicon nitride film.

8. The method of manufacturing the semiconductor device according to one of claims 1 to 7, wherein

said base impurity region (207, 211) has a first impurity region (207) and a second impurity region (211) of which impurity concentration is higher than that of said first impurity region,

said first and second impurity regions are formed at the main surface of said semiconductor substrate (1) such that said second impurity region surrounds a side surface of said first impurity region, and

said emitter impurity region (209) is formed within said first impurity region.

9. A semiconductor device comprising:

a semiconductor substrate (1) having a main surface;

a collector impurity region (3, 5, 13) of a first conductivity type formed at the main surface of said semiconductor substrate;

a base impurity region (7, 11: 207, 211) of a second conductivity type formed at the main surface of said semiconductor substrate within said collector impurity region;

an emitter impurity region (9: 209) of the first conductivity type formed at the main surface of said semiconductor substrate within said base impurity region; and

a conductive layer (15: 15a: 215: 215a) adjoining to said emitter impurity region,

said conductive layer having a polycrystalline silicon layer (15: 15b: 215: 215b) substantially uniformly doped with phosphorus at a concentration of at least  $1 \times 10^{20} \text{cm}^{-3}$ .

10. The semiconductor device according to claim 9, wherein said conductive layer (15: 215) is formed of a polycrystalline silicon layer doped with phosphorus, and

said phosphorus is contained in said polycrystalline silicon layer at a concentration of at most  $6 \times 10^{20} \text{cm}^{-3}$ .

11. The semiconductor device according to claim 9, wherein said conductive layer (15a: 215a) has a polycrystalline silicon layer (15b: 215b) doped with phosphorus and a silicide layer (15c: 215c) formed on said polycrystalline silicon layer, and  
said phosphorus is contained in said polycrystalline silicon layer at a concentration of at most  $1 \times 10^{21} \text{cm}^{-3}$ .
12. The semiconductor device according to one of claims 9 to 11, further comprising:  
a first insulating layer (101) formed on the main surface of said semiconductor substrate (1);  
a second insulating layer (103) formed on said first insulating layer and having different etch characteristic than said first insulating layer; and  
a third insulating layer (63) formed on said second insulating layer having different etch characteristic than said second insulating layer; wherein  
said first, second and third insulating layers have an aperture (163a<sub>2</sub>: 262d) reaching said emitter impurity region (9: 209), and  
said conductive layer (15: 15a: 215: 215a) is in contact with said emitter impurity region through said aperture.
13. The semiconductor device according to claim 12, wherein  
said first and third insulating layers (101, 63) each include a silicon oxide film, and said second insulating layer (103) includes a silicon nitride film.

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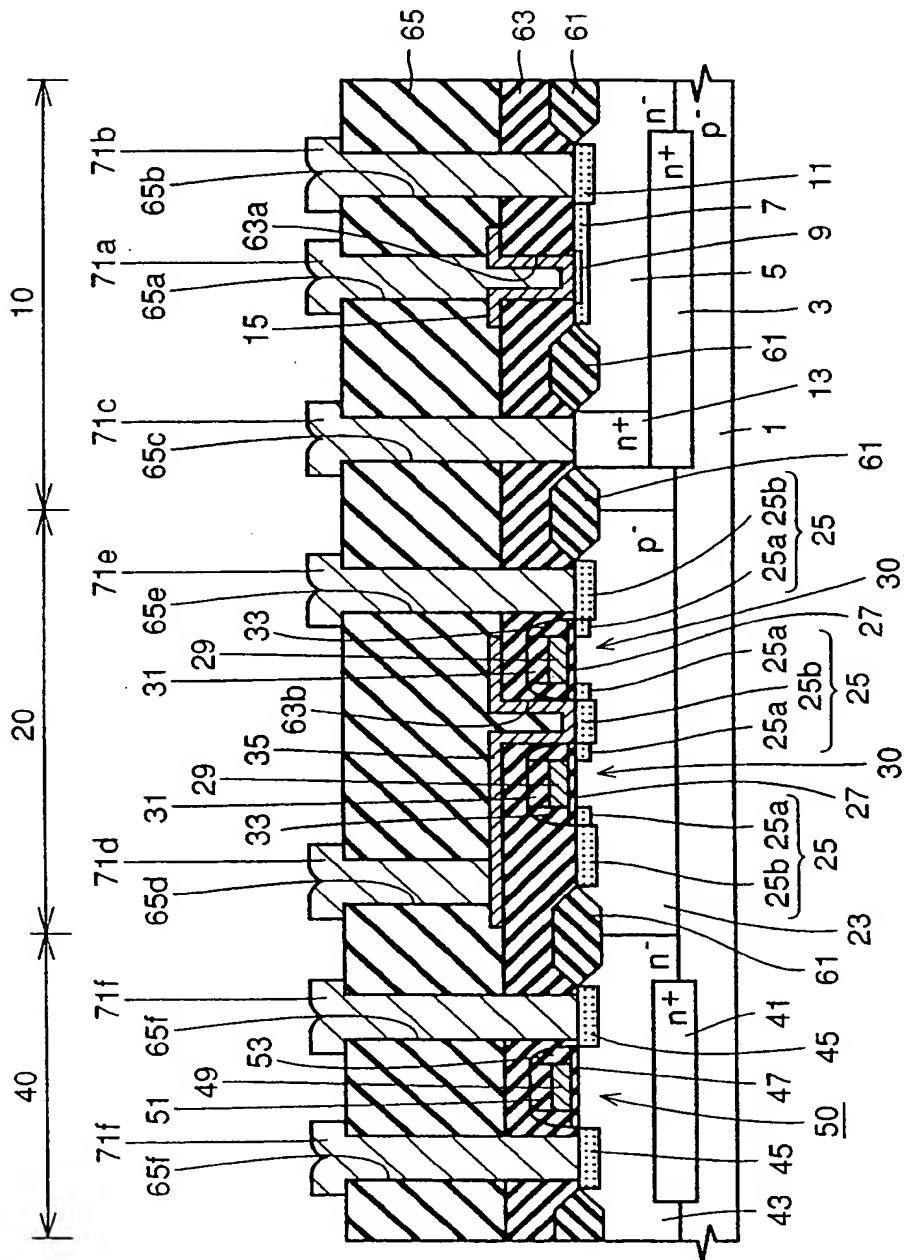
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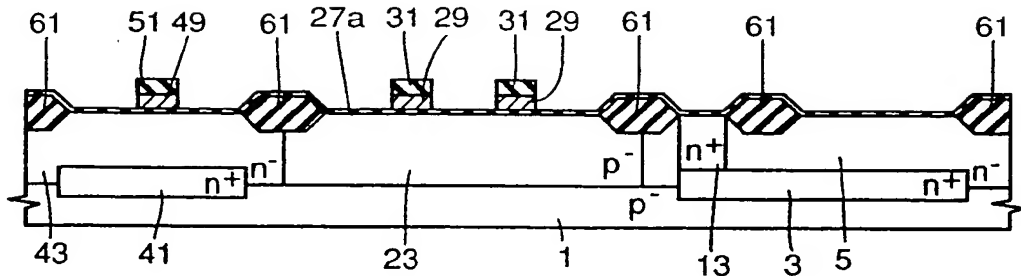
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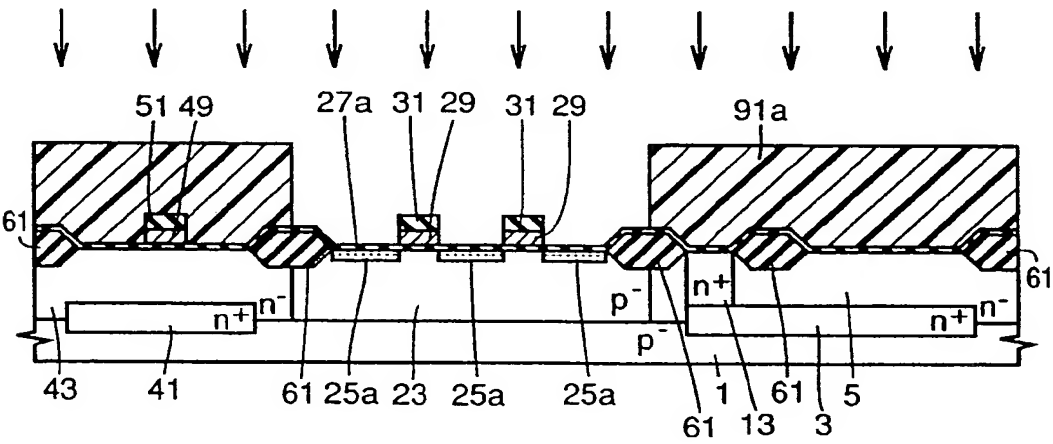
FIG.1



*FIG.2*



**FIG.3**



**FIG.4**

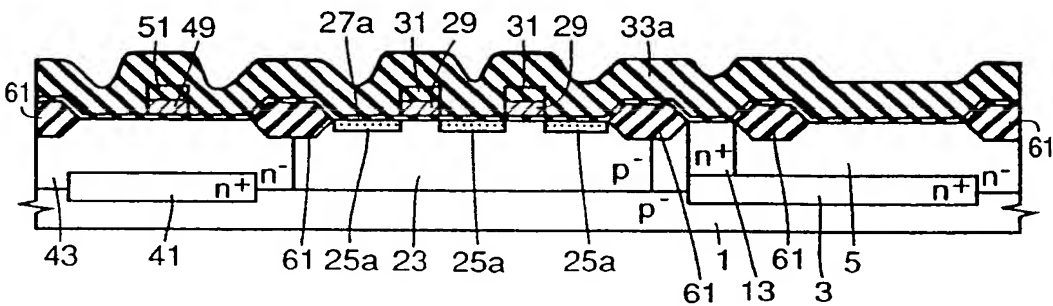




FIG.5

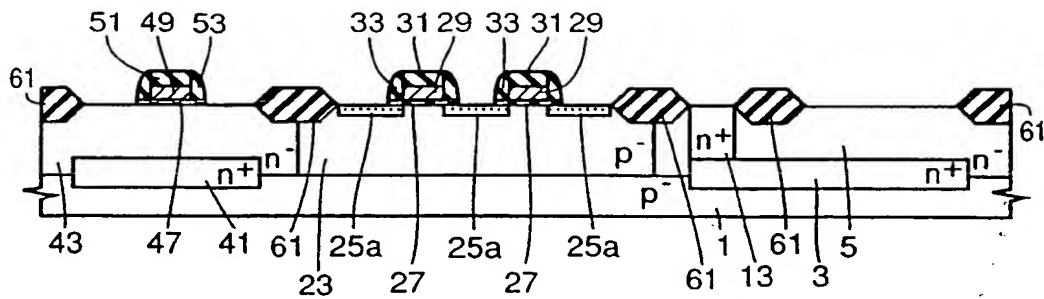


FIG.6

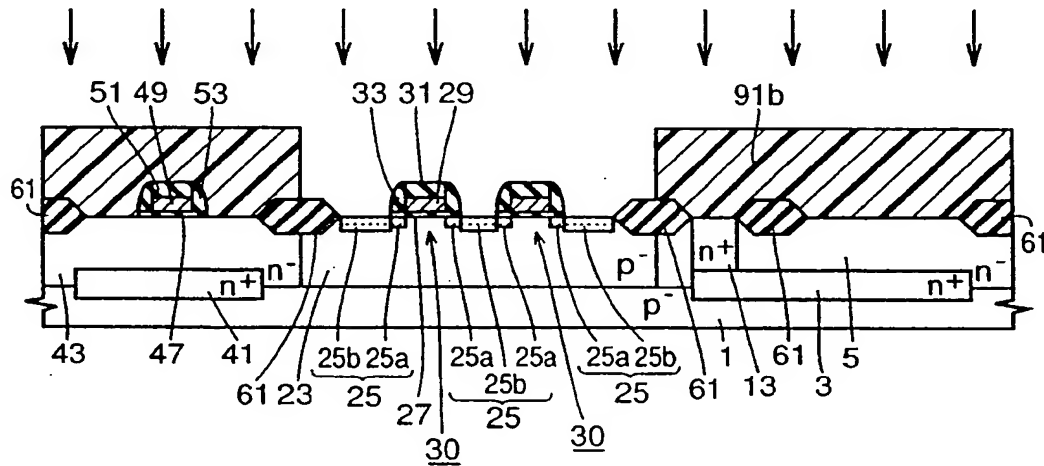
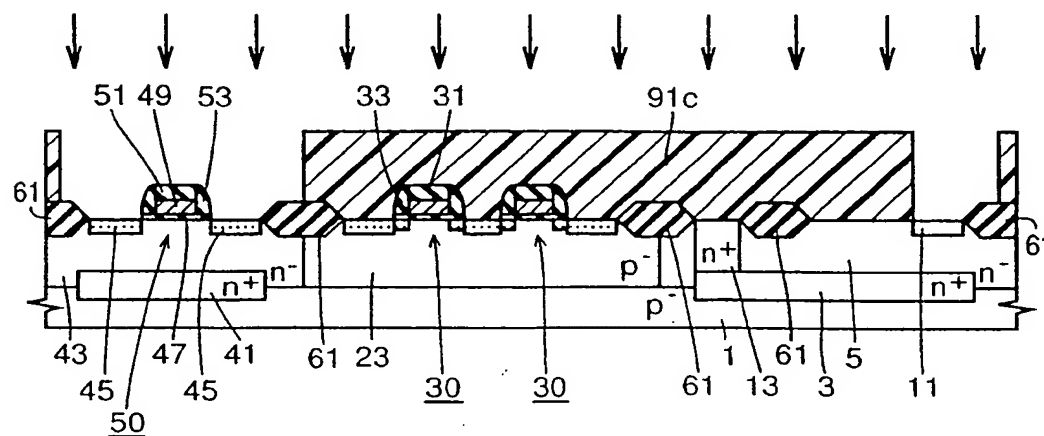
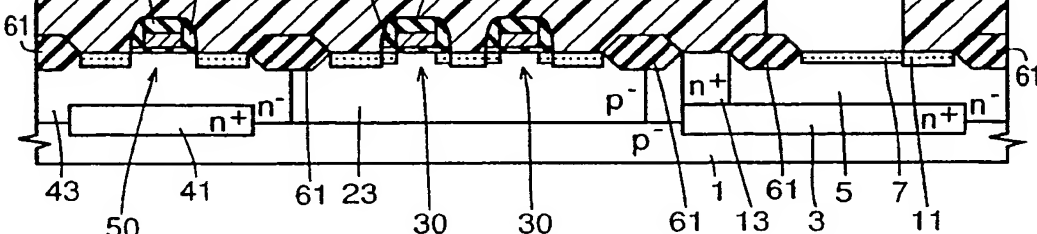
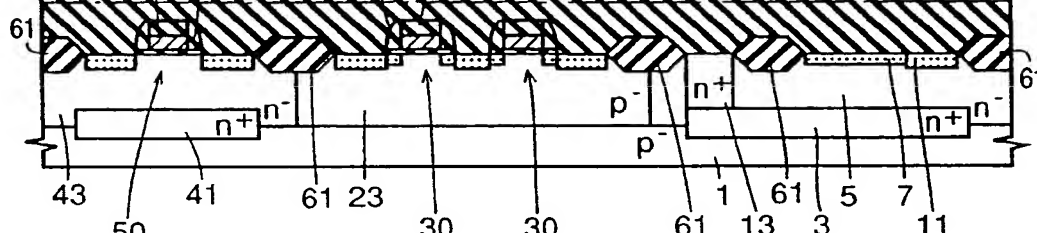


FIG.7





51 53 67 33 31 63a<sub>0</sub>



A cross-sectional view of a substrate 63 with a patterned layer 31 on its top surface. The patterned layer 31 consists of a series of rectangular blocks 33 separated by gaps 53. The gaps 53 are wider than the blocks 33. The label 51 points to the top surface of the blocks 33.

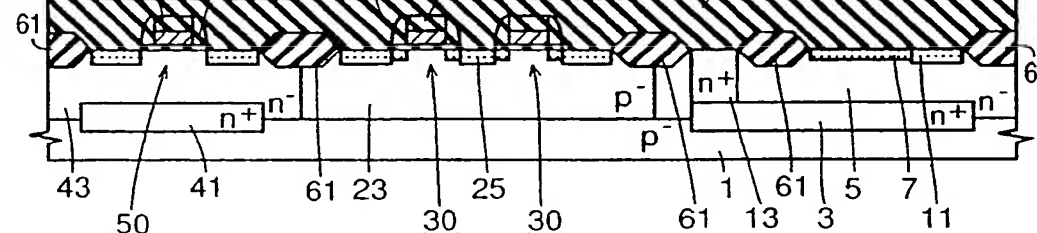


FIG. 11

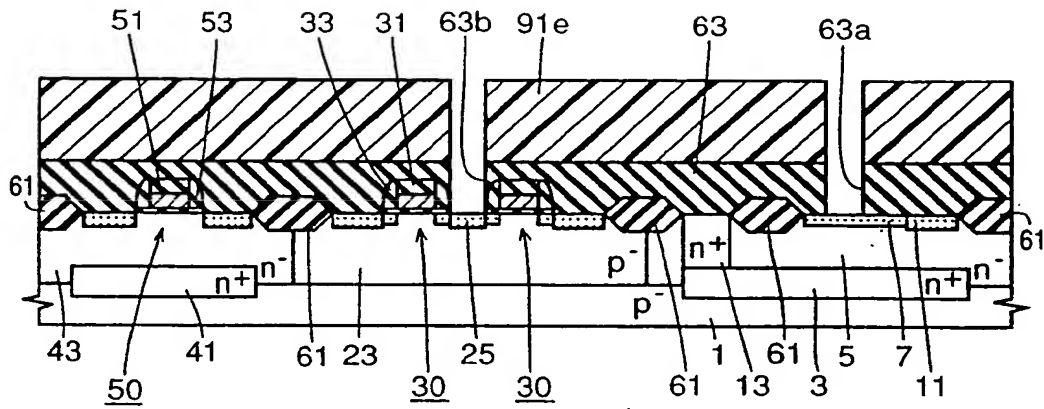


FIG. 12

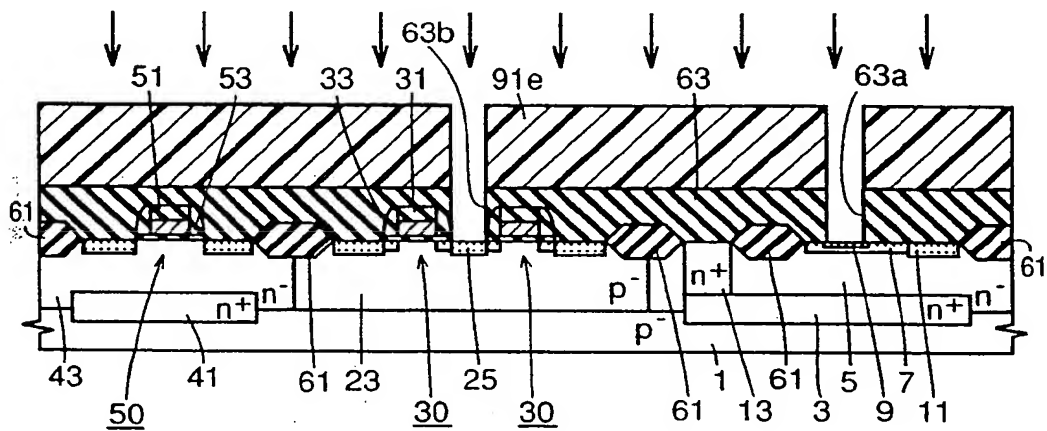


FIG. 13

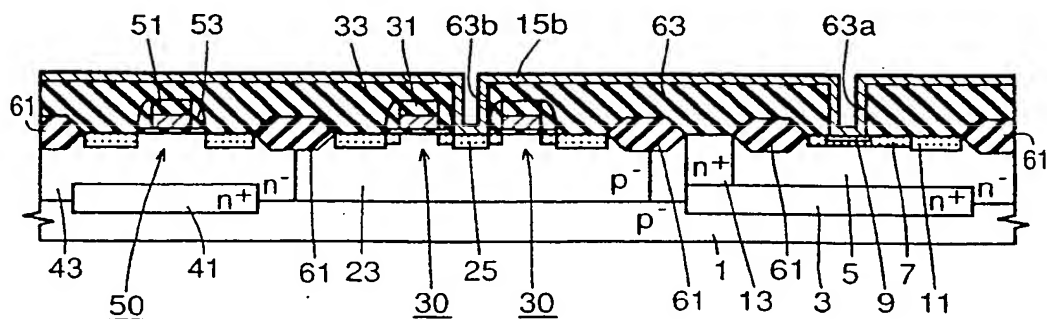


FIG. 14

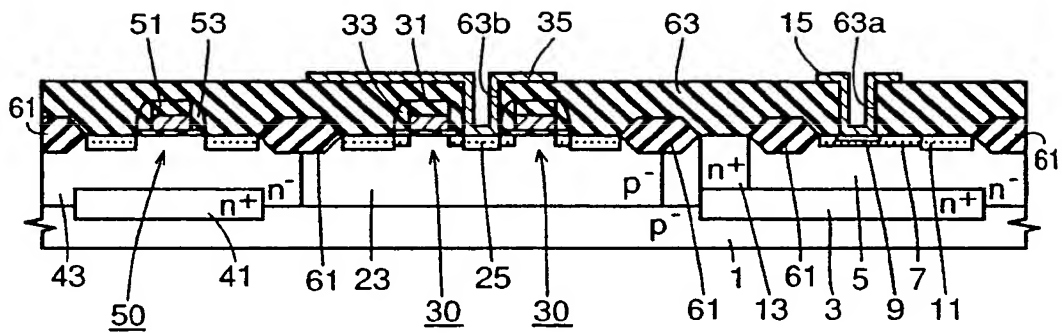


FIG. 15

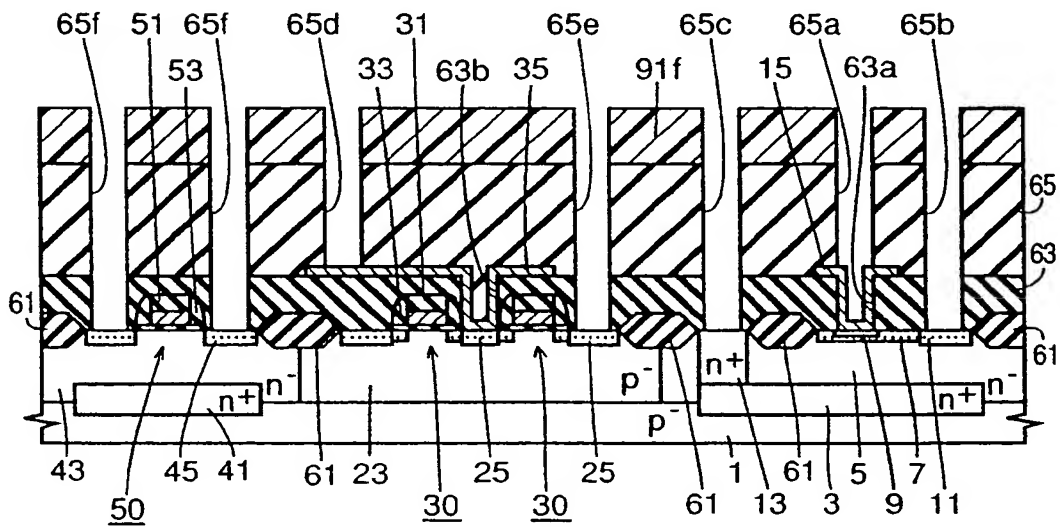


FIG. 16

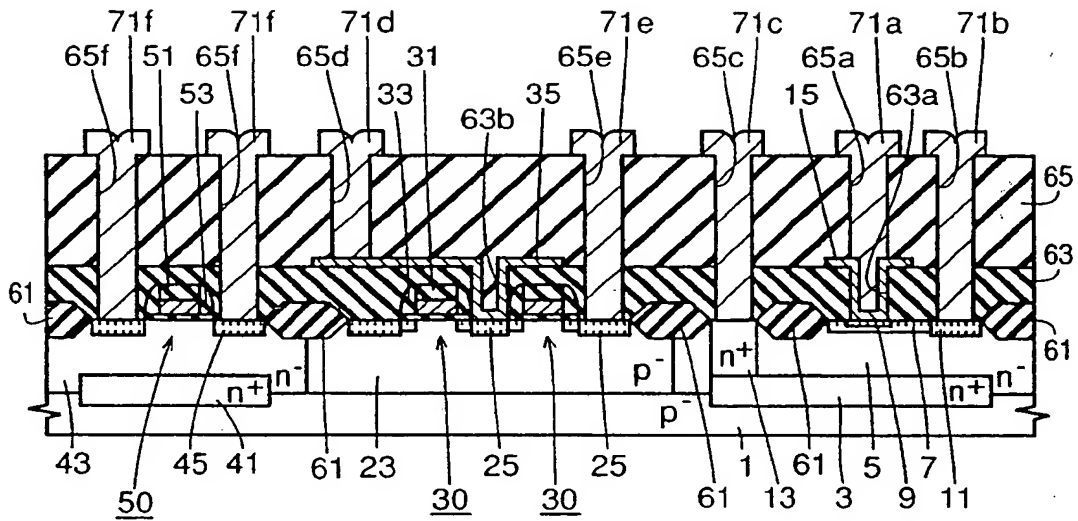


FIG. 17

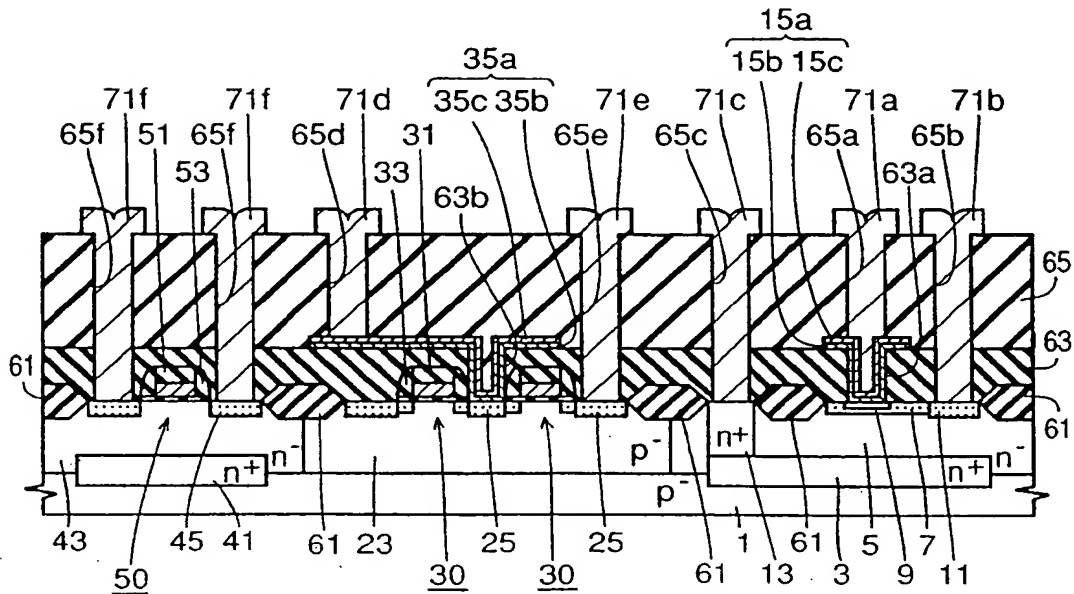


FIG. 18

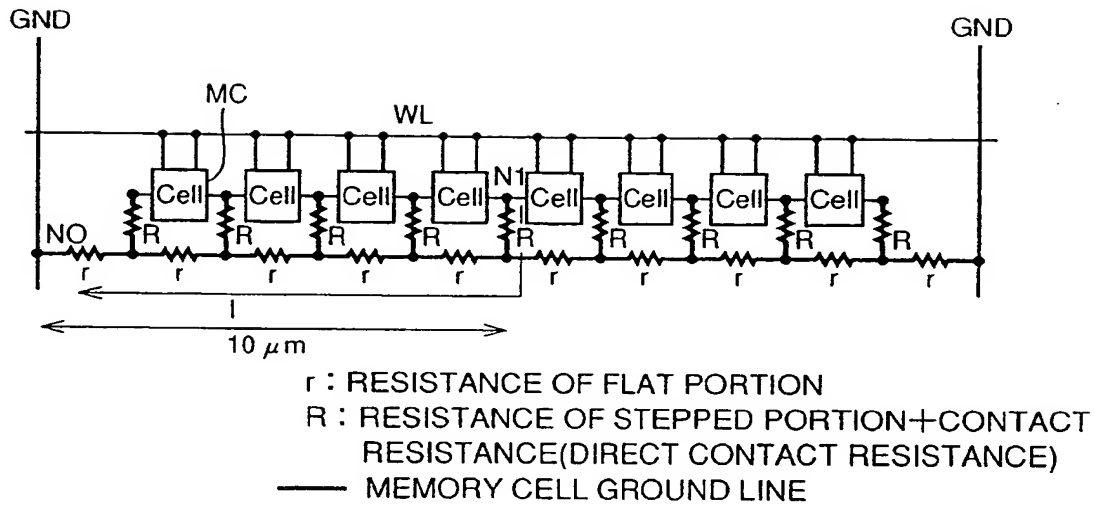


FIG. 19

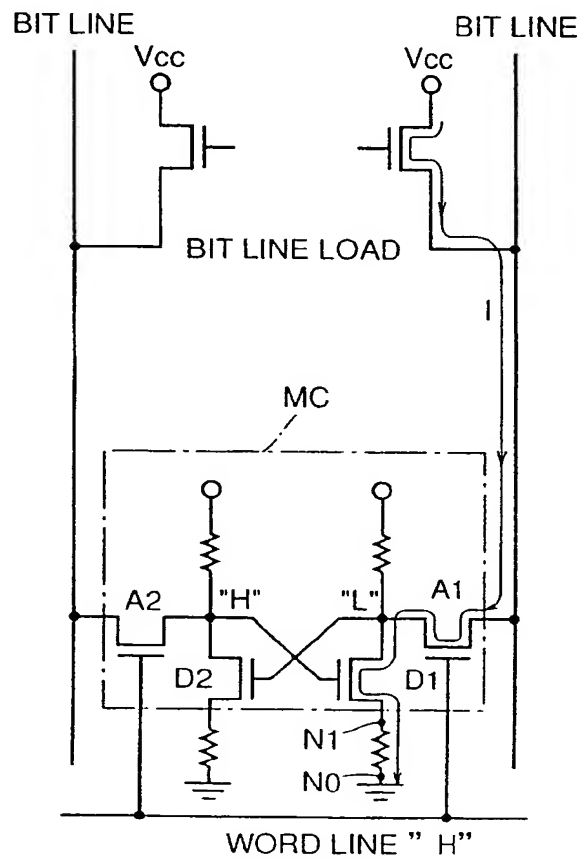


FIG.20

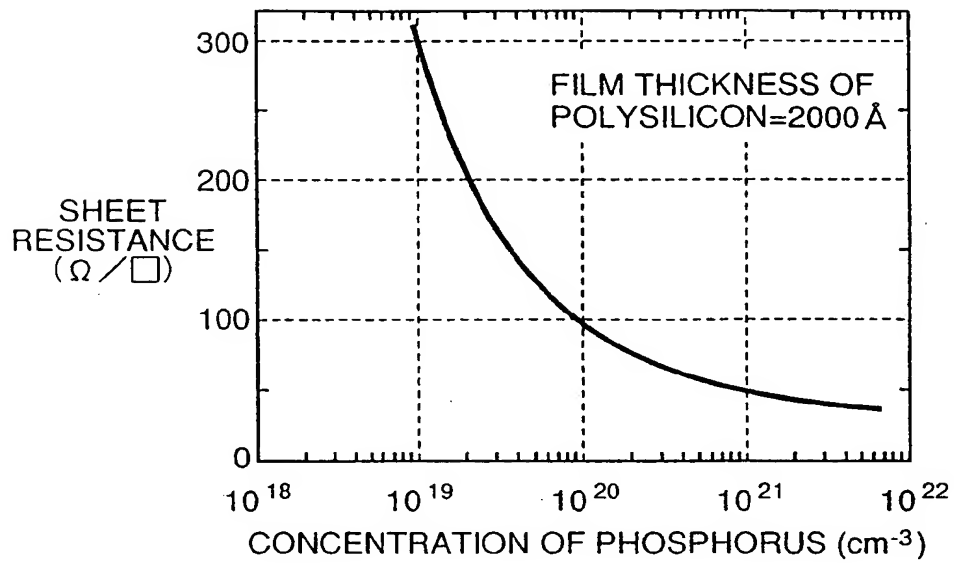


FIG.21

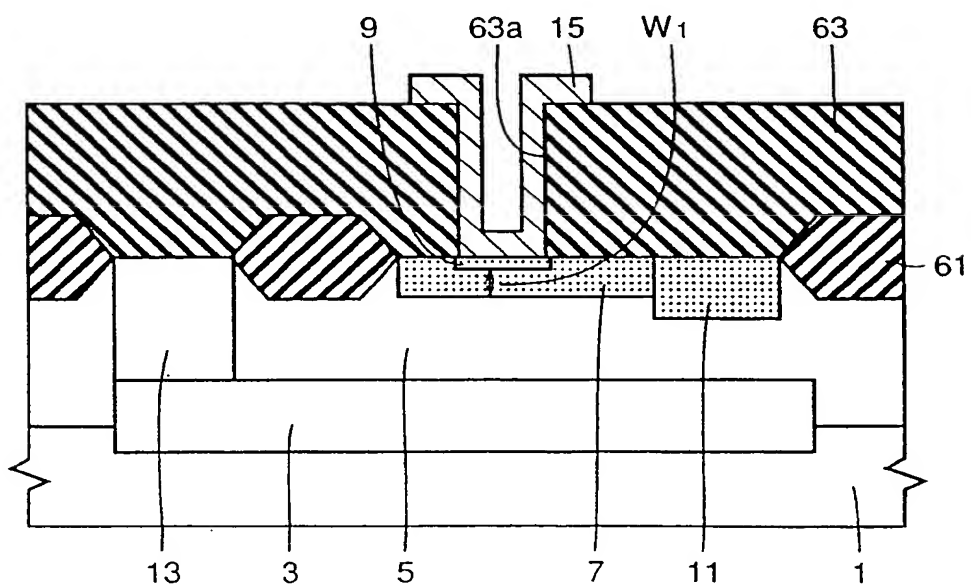




FIG.22

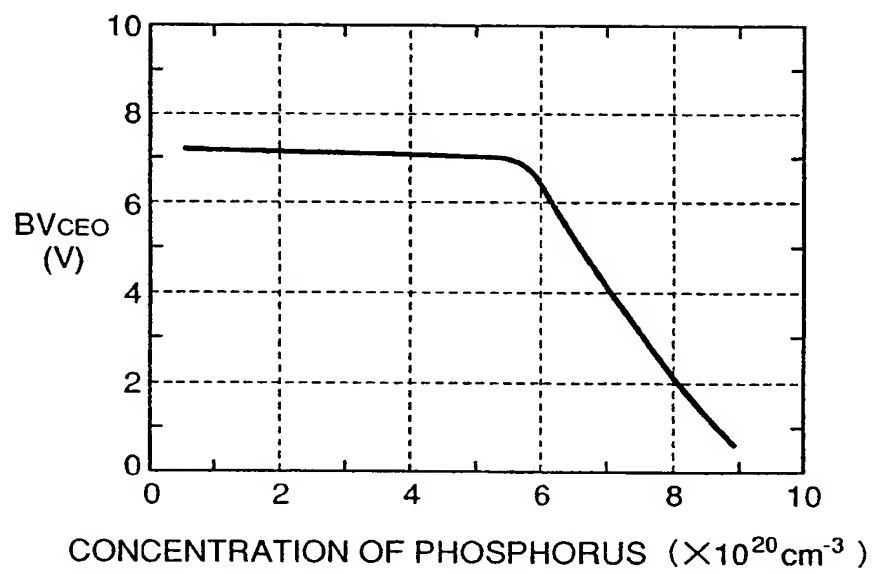


FIG.23

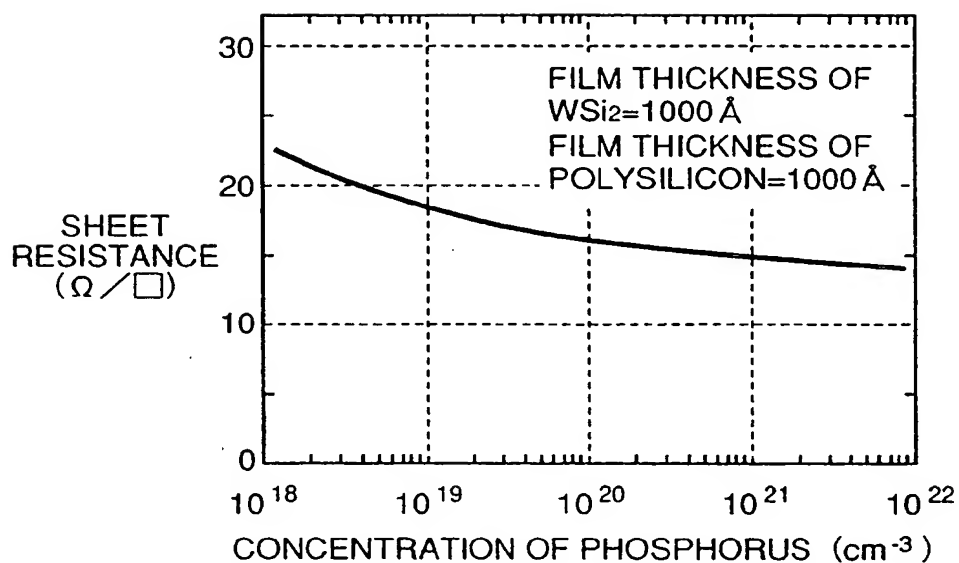


FIG.24

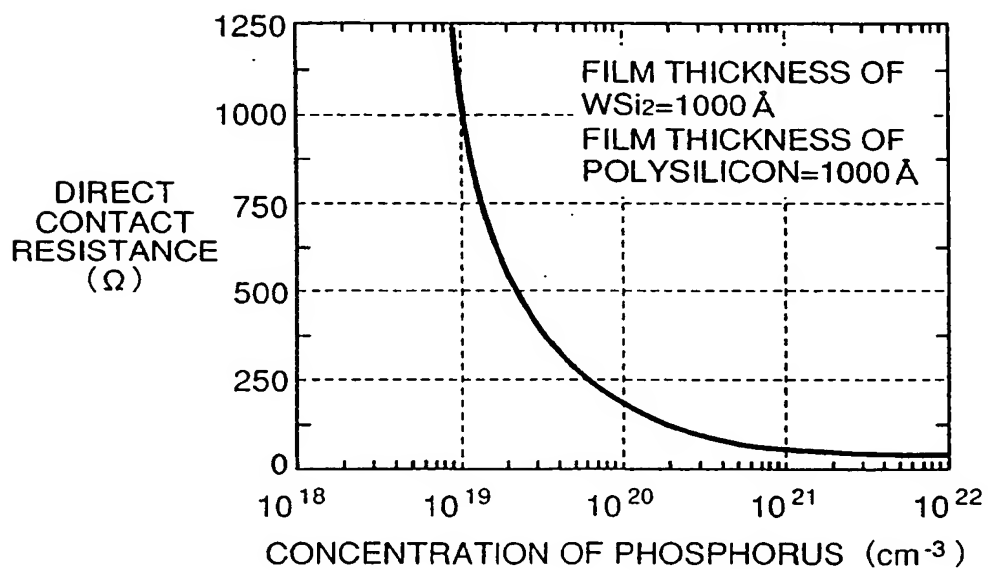


FIG.25

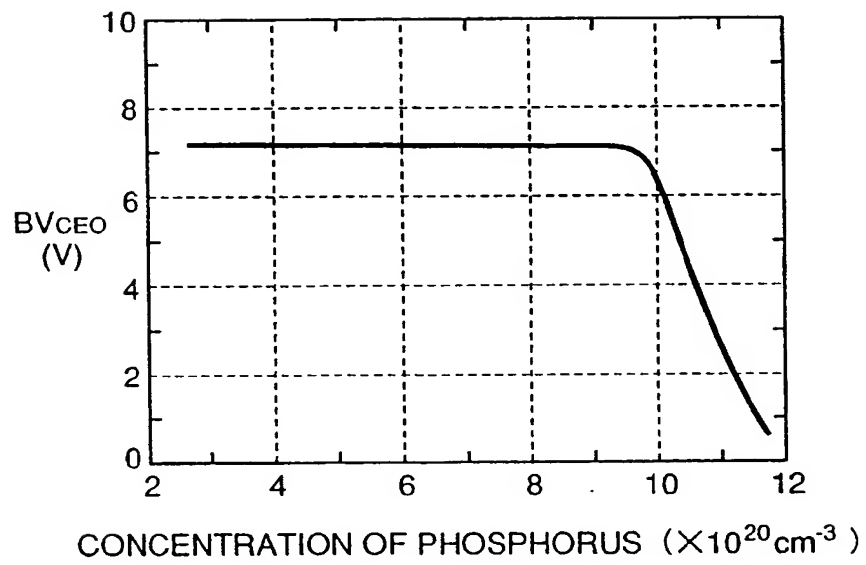


FIG. 26

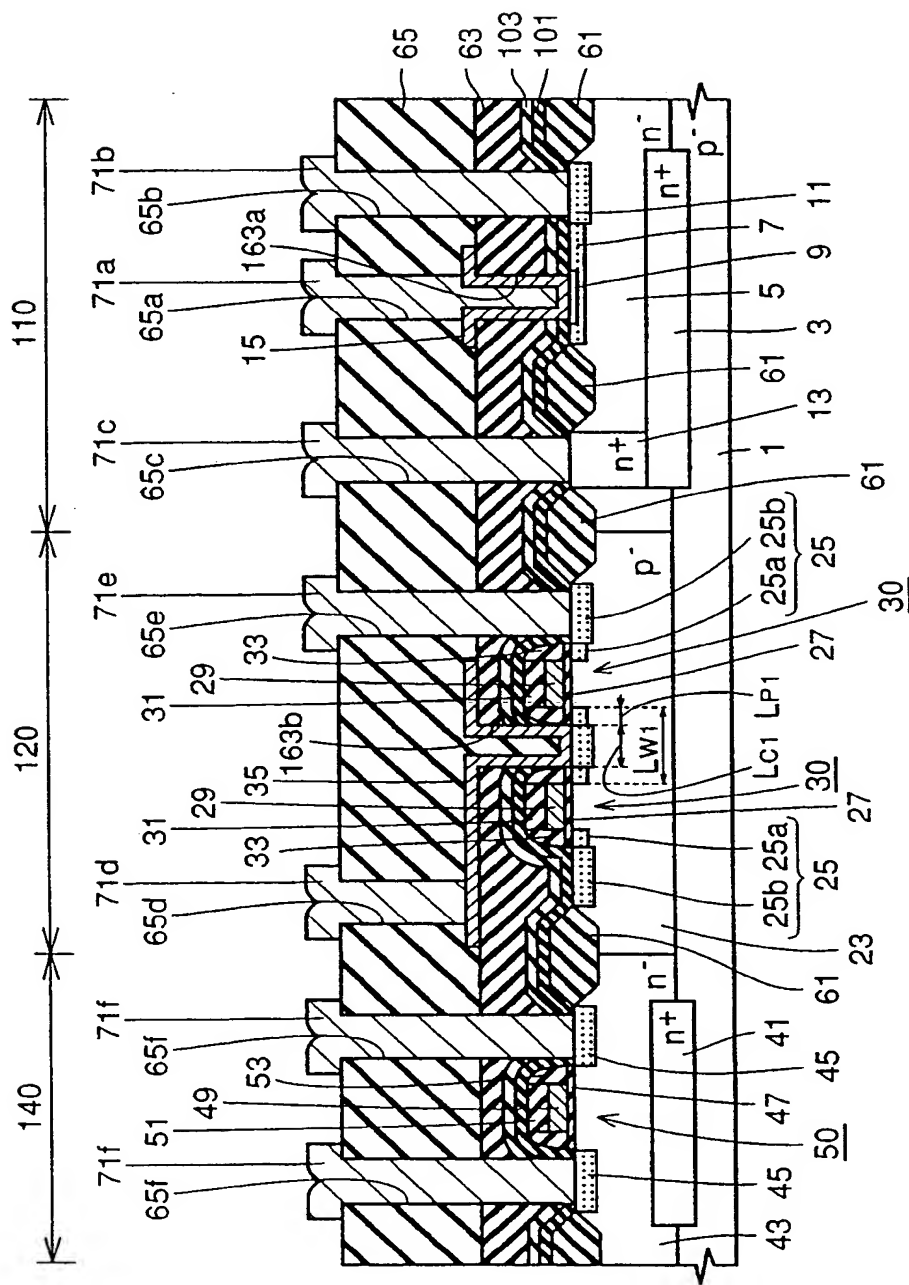






FIG.33

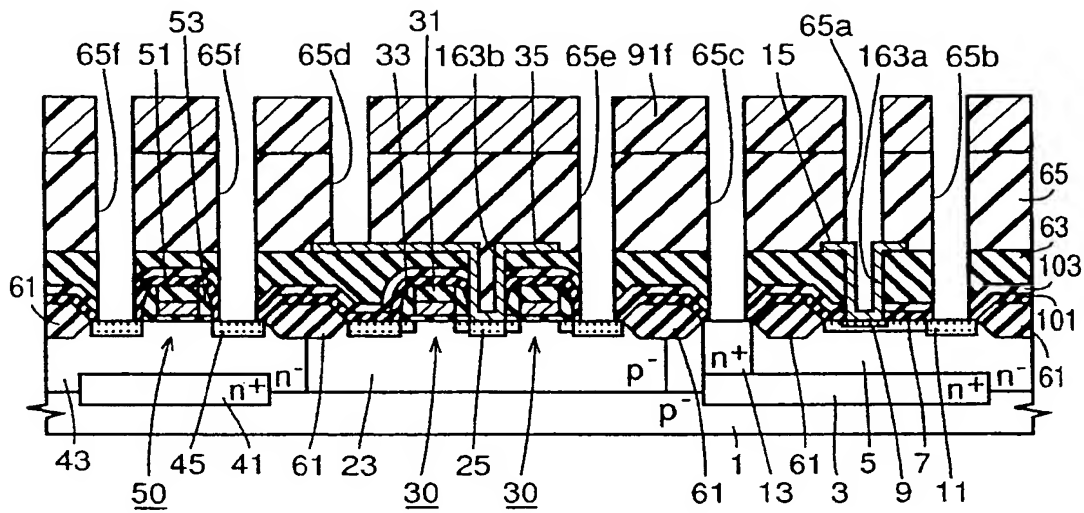


FIG.34

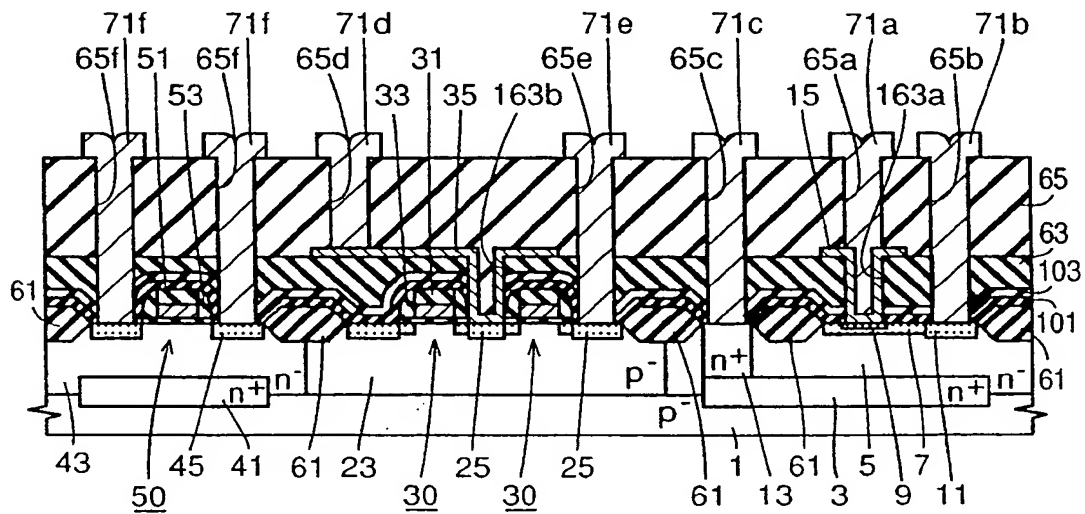




FIG.35

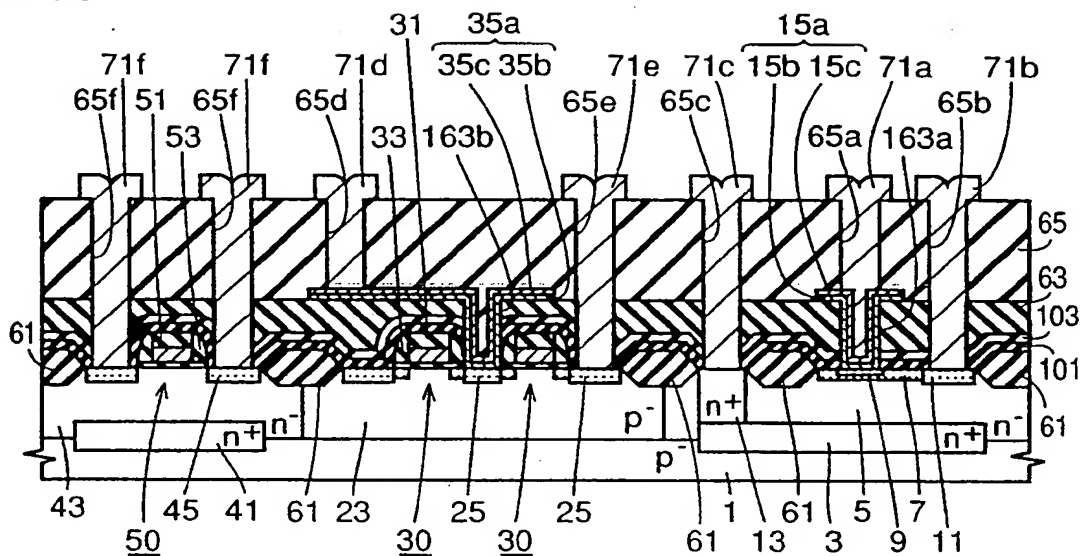


FIG.36

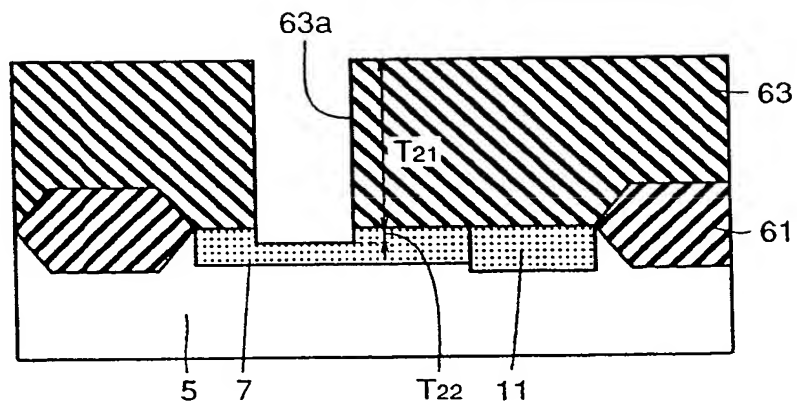


FIG.37

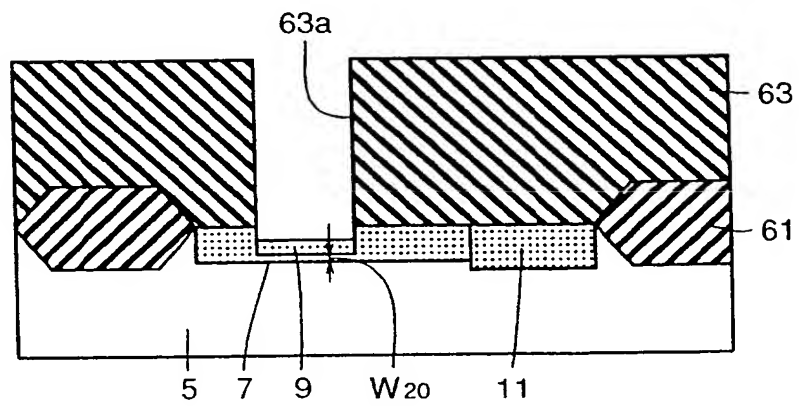


FIG.38

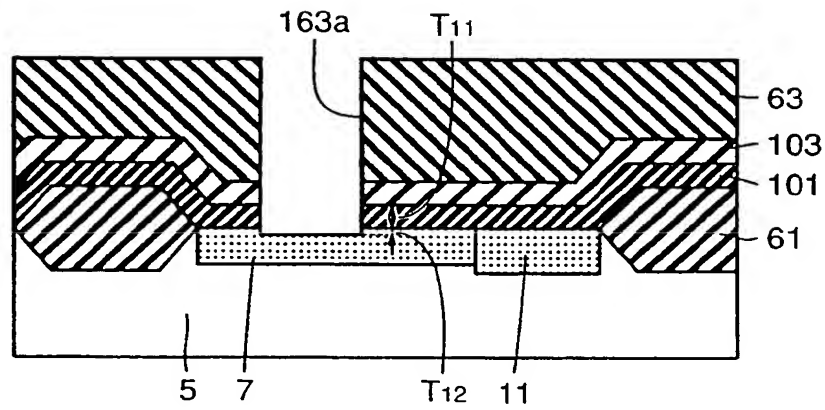


FIG.39

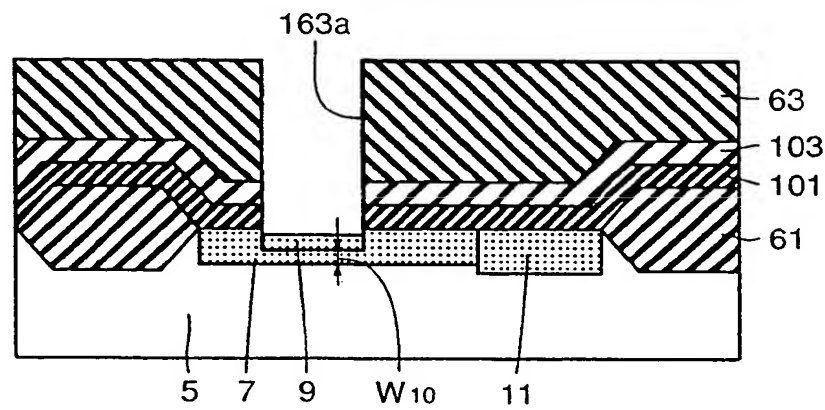


FIG. 40

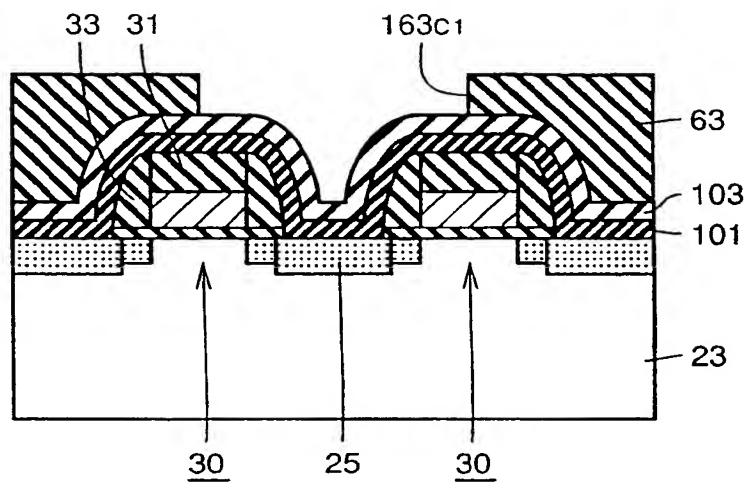


FIG. 41

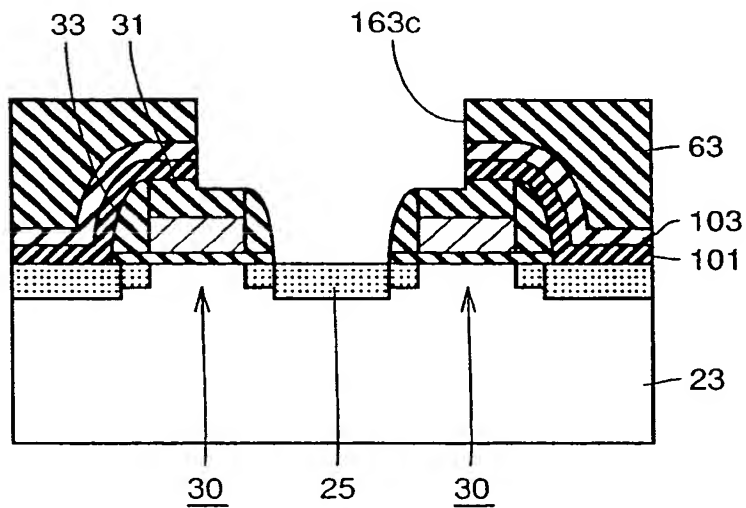


FIG.42

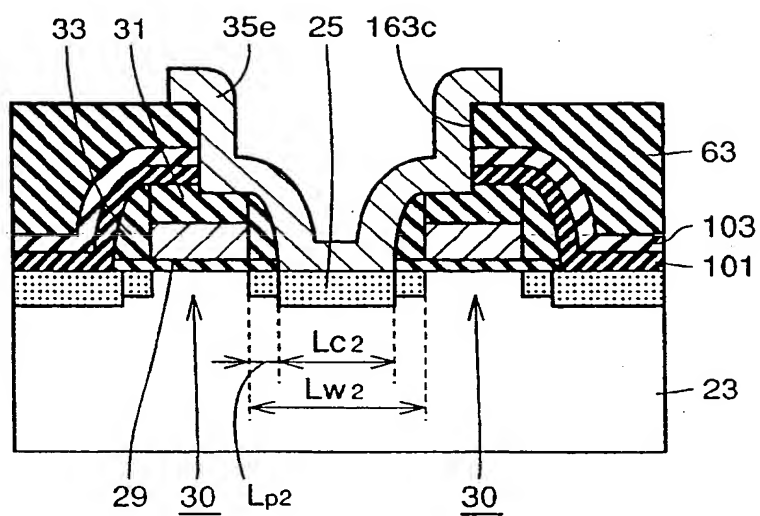


FIG. 43

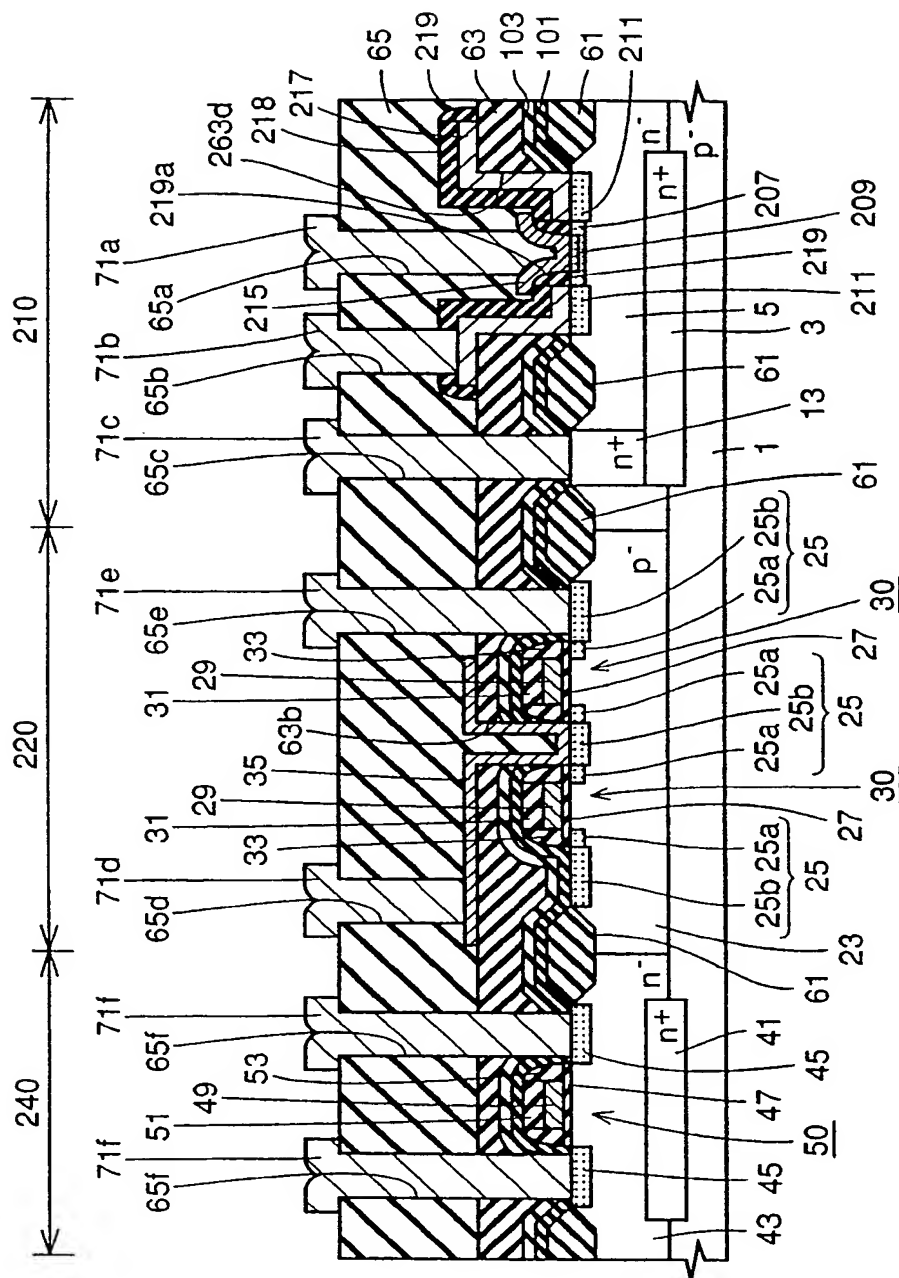




FIG. 46

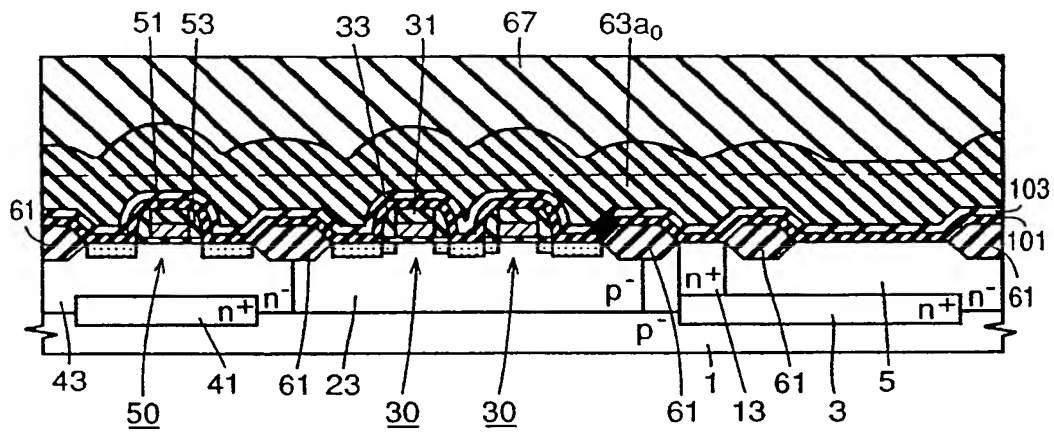


FIG. 47

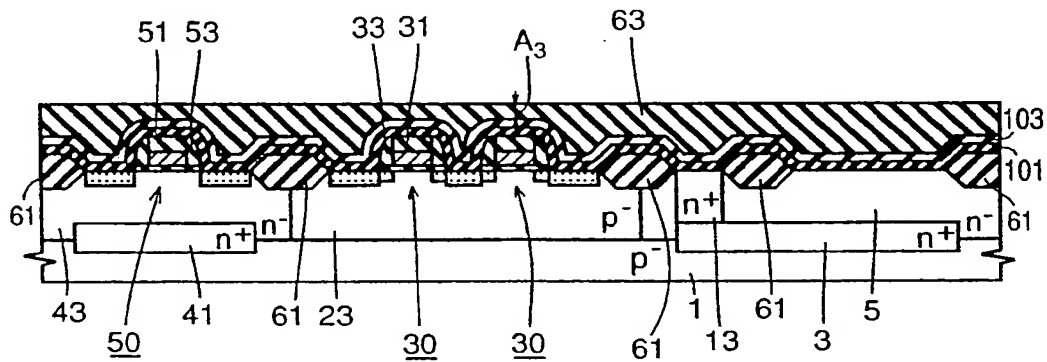


FIG. 48

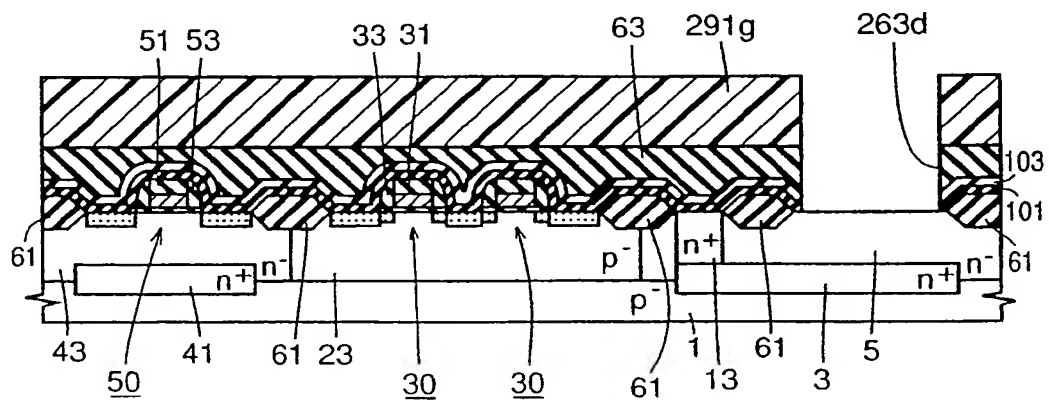




FIG.49

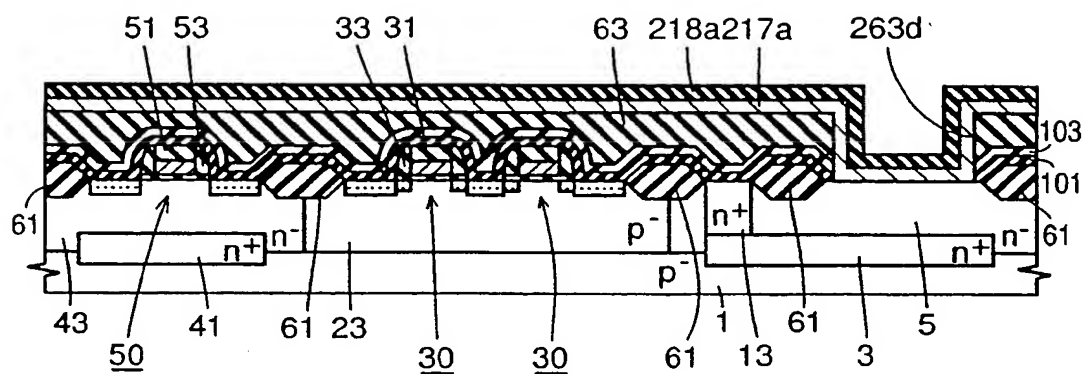


FIG.50

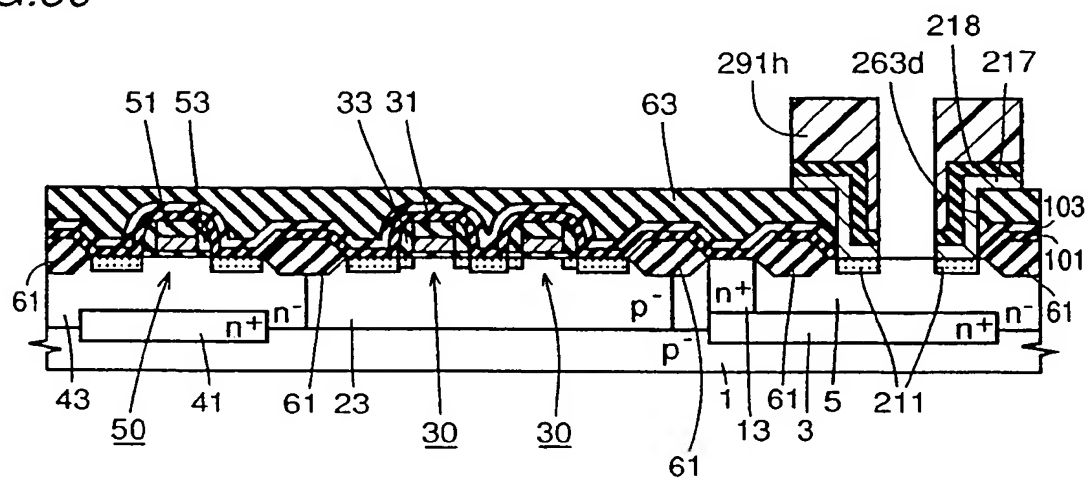


FIG.51

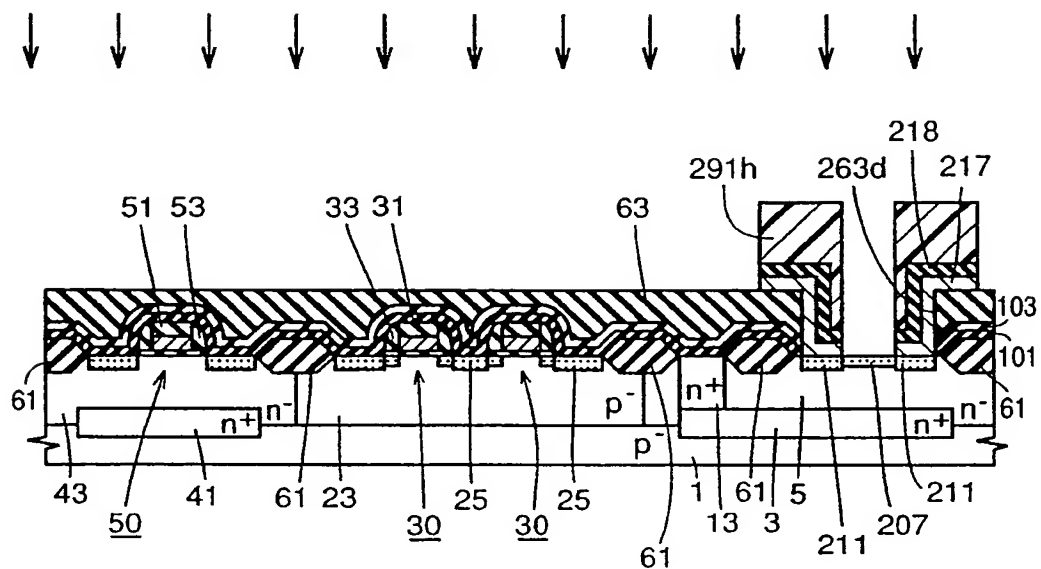
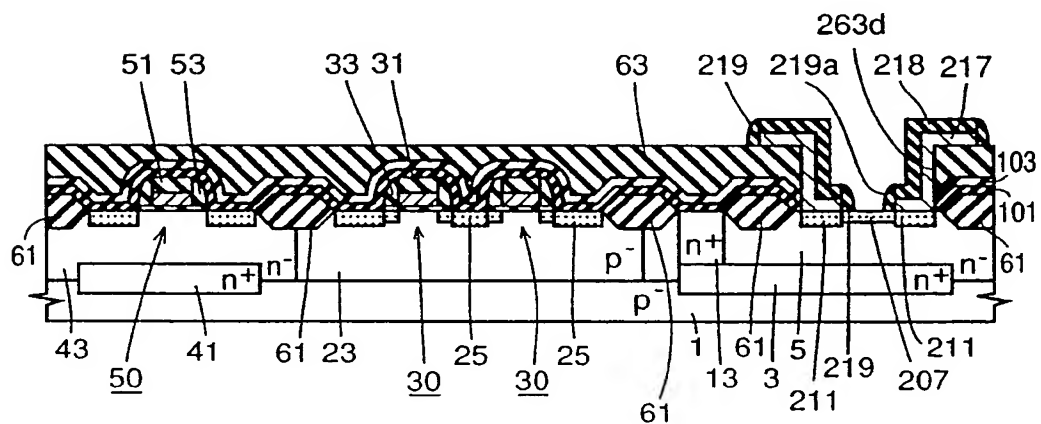


FIG.52





A detailed cross-sectional view of a semiconductor device. The structure consists of a substrate with alternating  $n^+$  and  $n^-$  regions, and a  $p^-$  region. Various layers and structures are labeled with numbers: 43, 50, 41, 61, 23, 30, 25, 30, 25, 1, 61, 13, 3, 219, 207, 209, 211, 219, 211, 219, 219a, 263d, 217, 103, 101, 61, 51, 53, 33, 31, 63b, 15b, 63, 218. The diagram shows a complex arrangement of these layers, including a top layer with a hatched pattern, and various internal structures like a central  $n^+$  region and a  $p^-$  region.

A detailed cross-sectional view of a semiconductor device. The substrate consists of alternating layers of  $n^+$  and  $p^-$  regions. A series of gates, labeled 31, 33, 35, and 63b, are positioned on the surface. These gates are connected to a common line 63. Various contacts and interconnects are shown, including 51, 53, 61, 101, 103, 217, 218, 219, 219a, 215, 263d, 211, 207, 209, 13, 3, 5, 25, 23, 41, 43, and 50. The device is shown in a perspective view, with some components like 219 and 219a appearing as raised structures.

FIG. 57

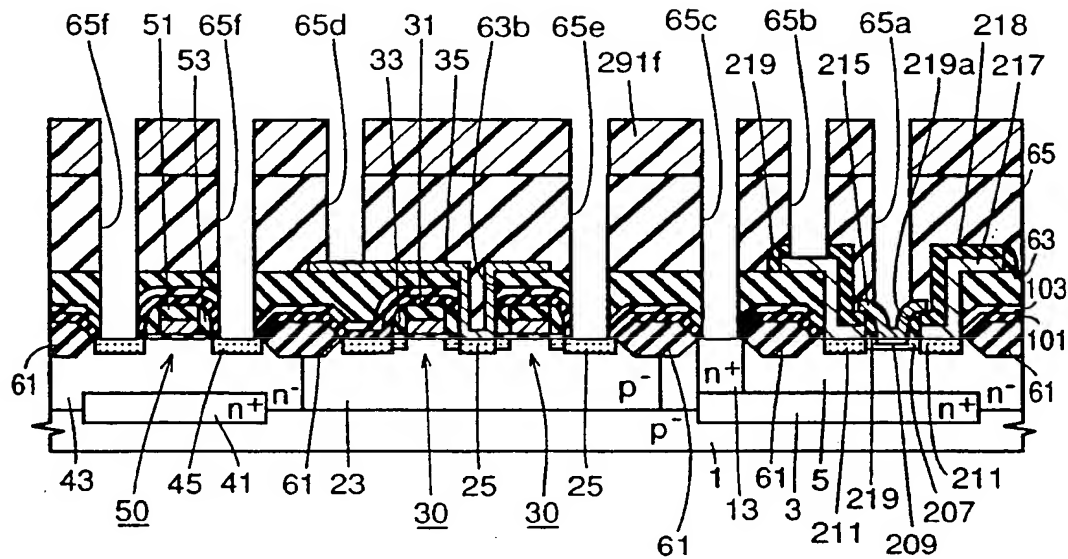


FIG. 58

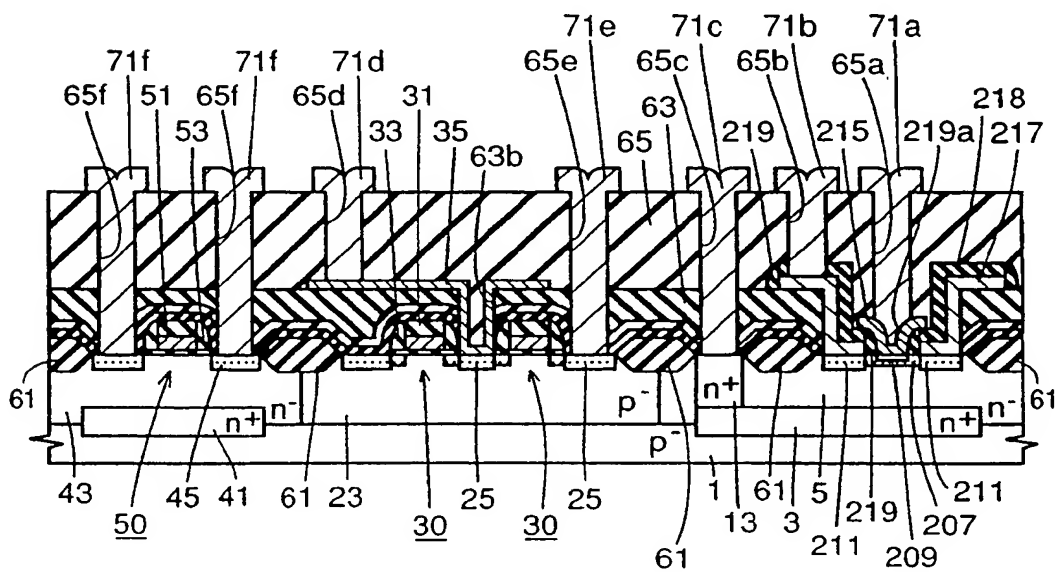


FIG.59

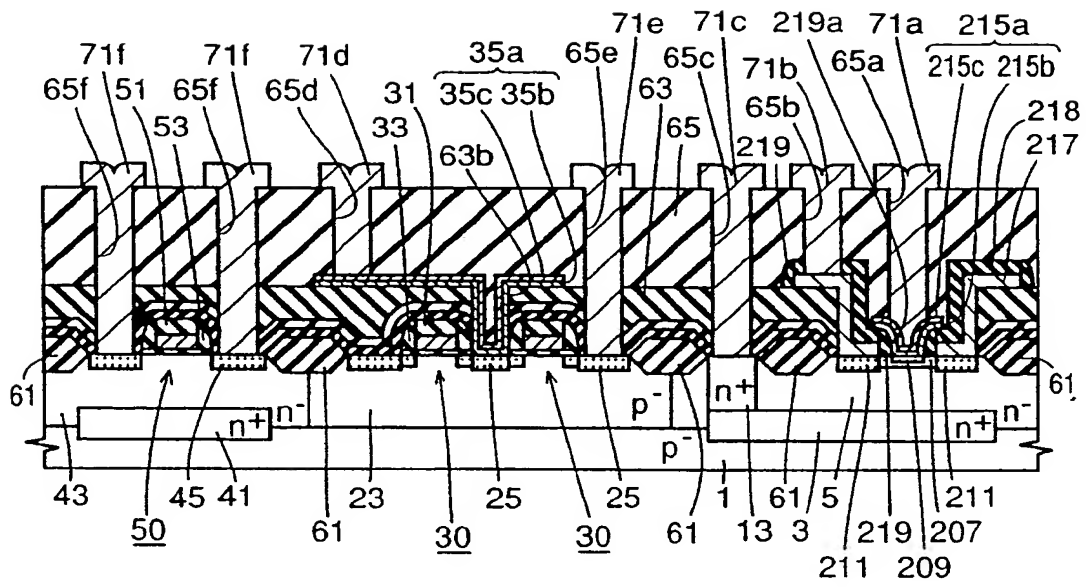


FIG. 60

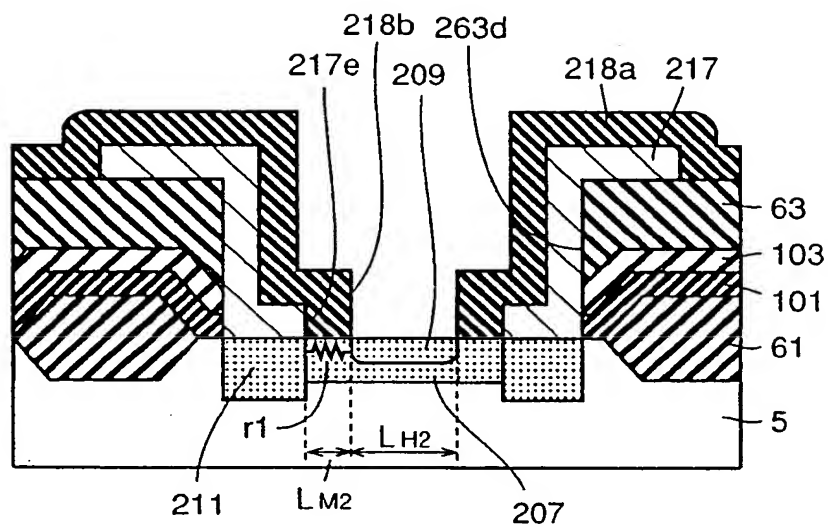


FIG. 61

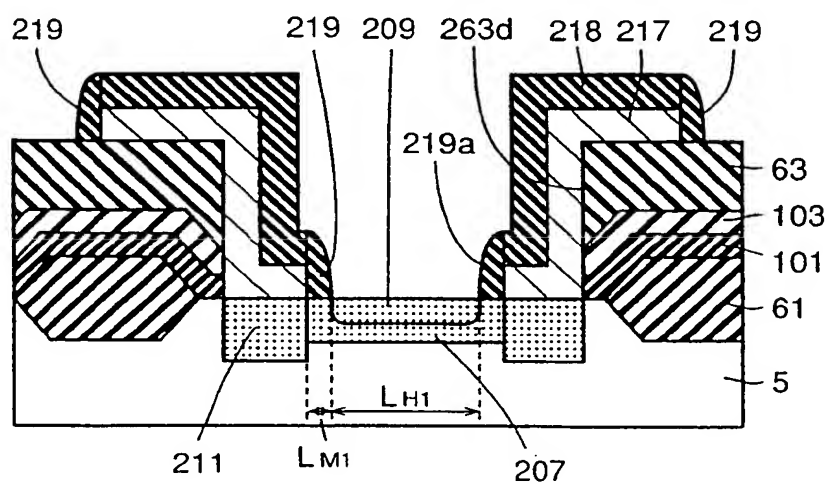


FIG.62

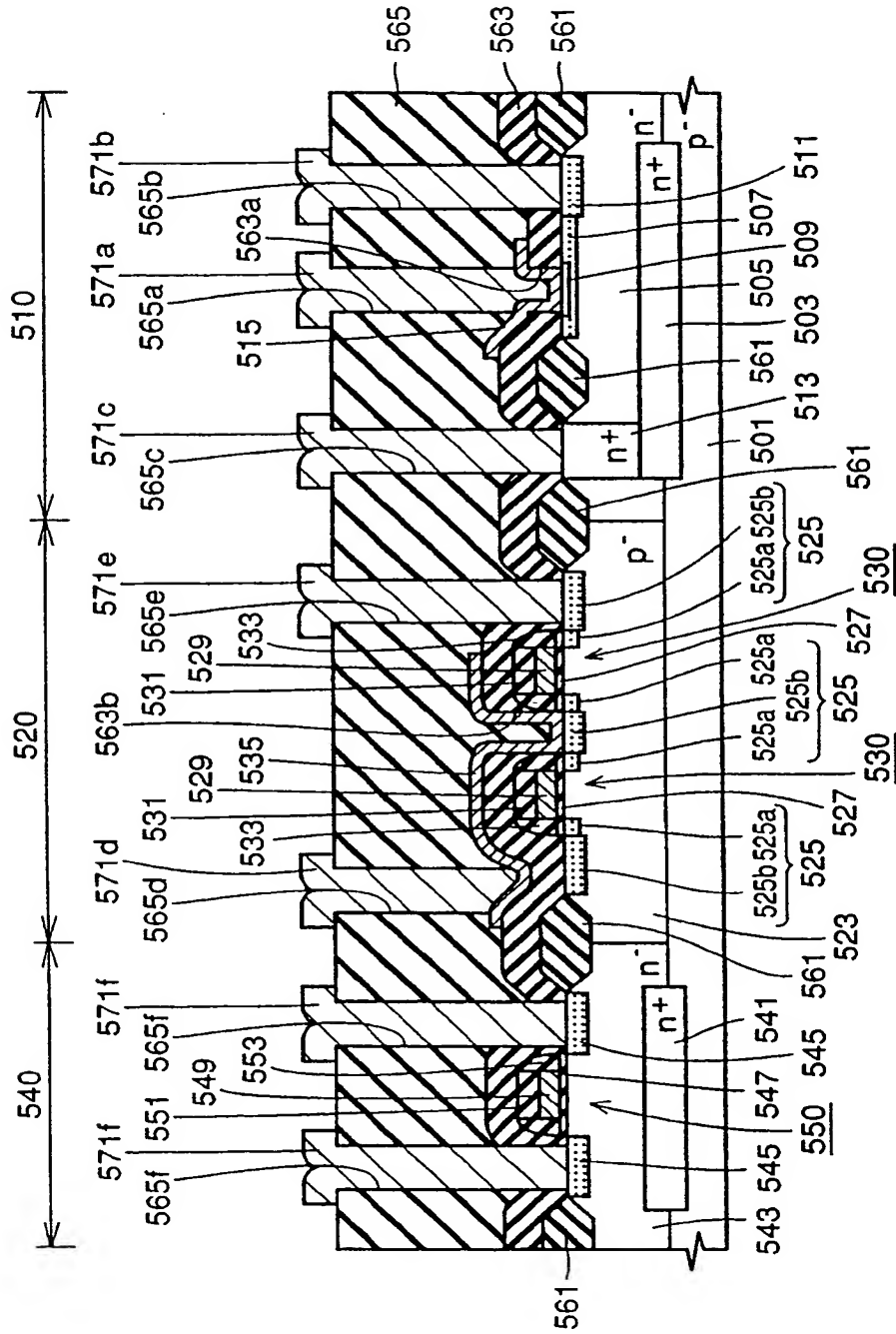




FIG.63

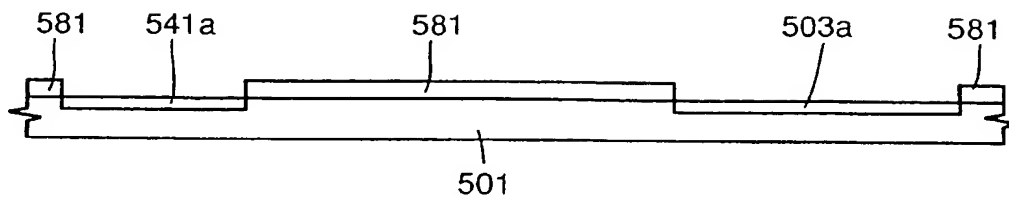


FIG.64

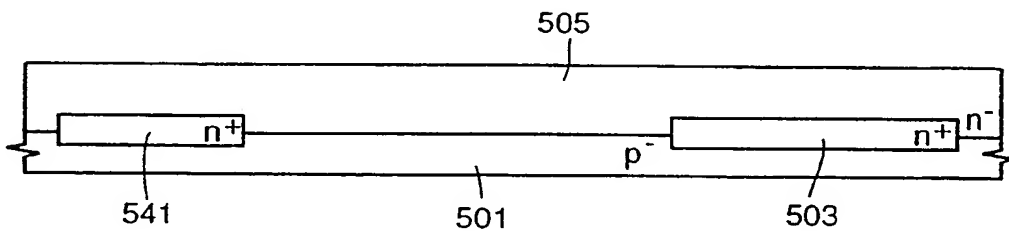


FIG.65

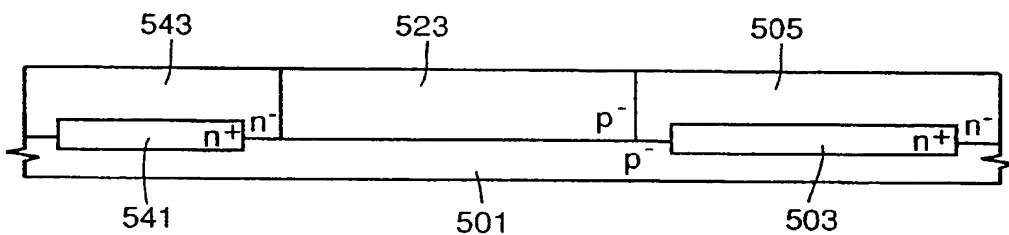
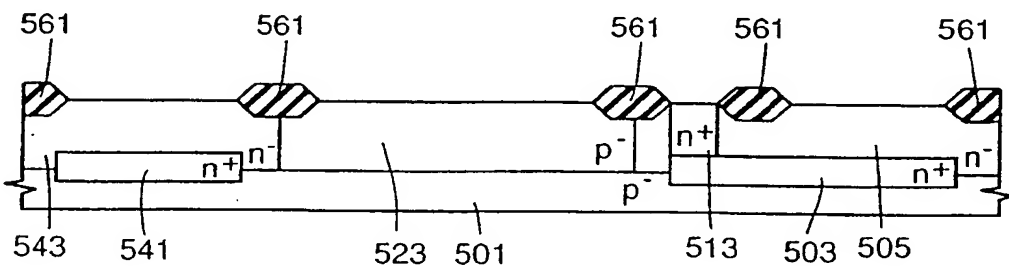


FIG.66



8

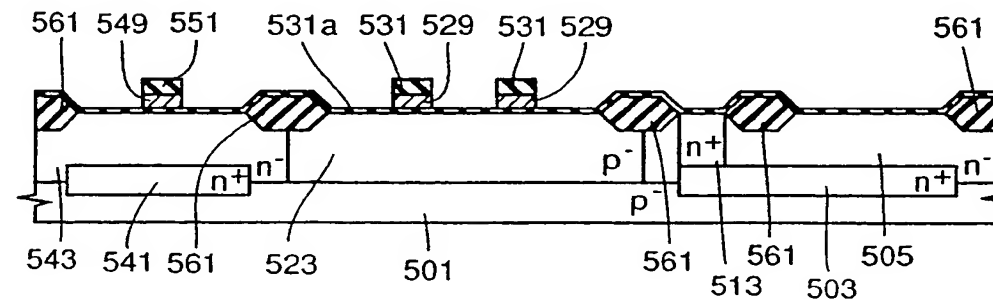
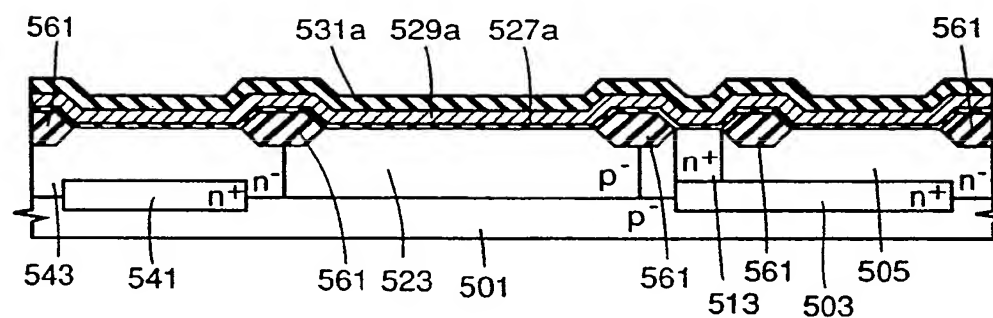
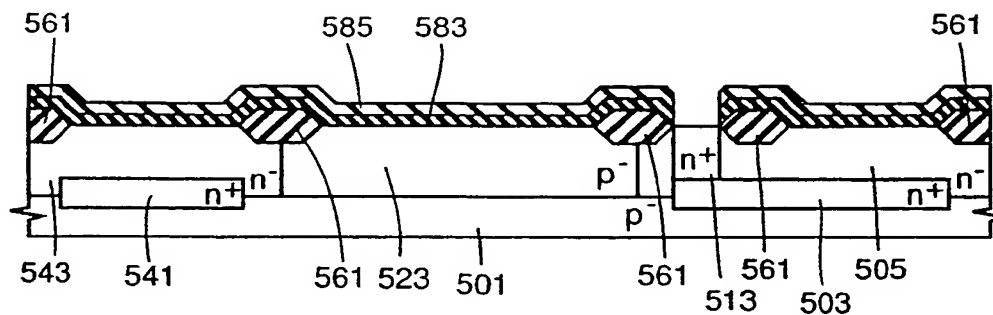


FIG. 70

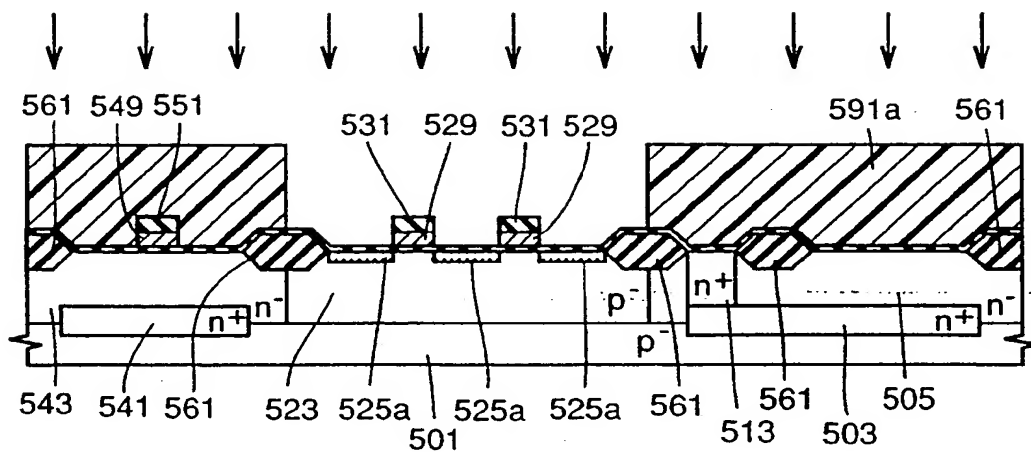


FIG. 71

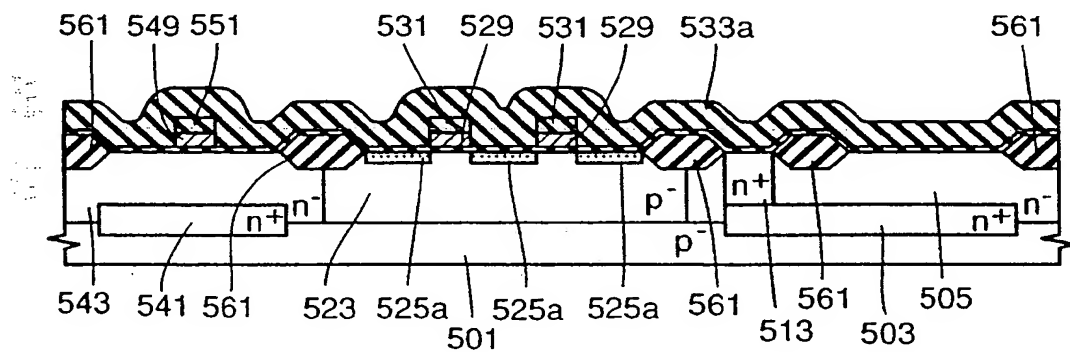


FIG. 72

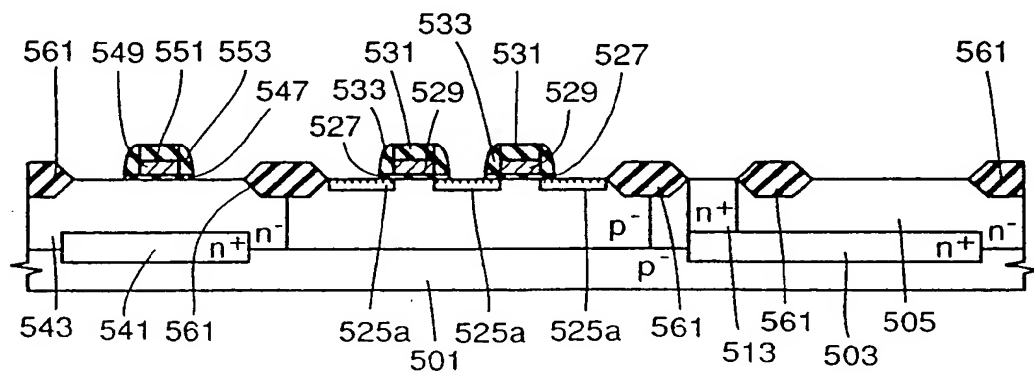


FIG.73

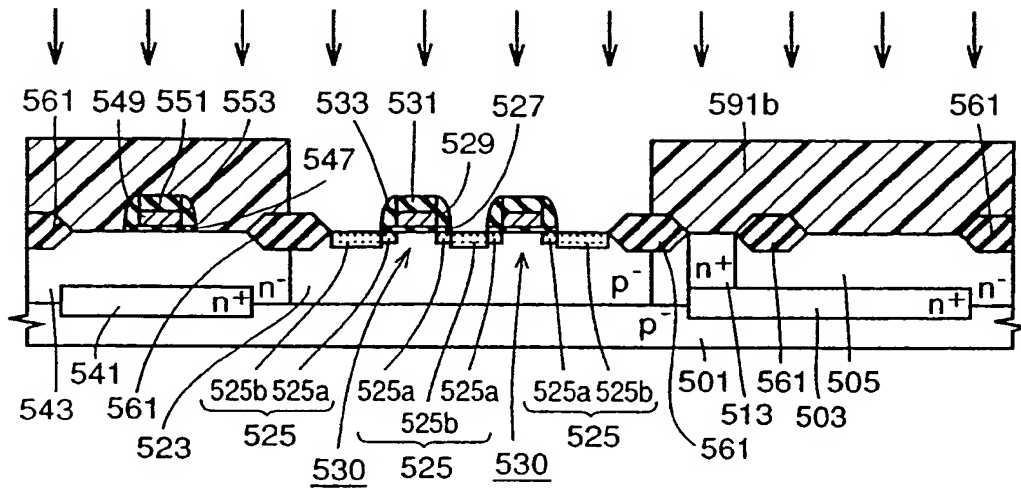


FIG.74

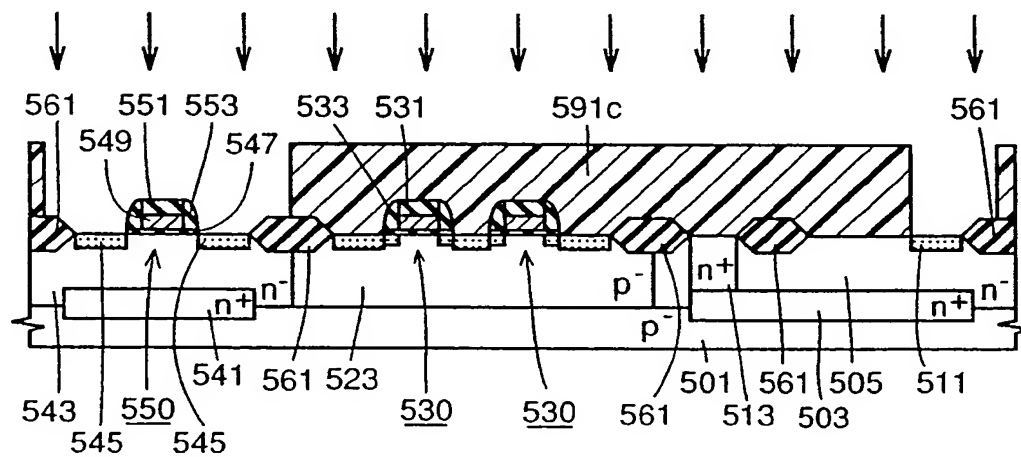


FIG.75

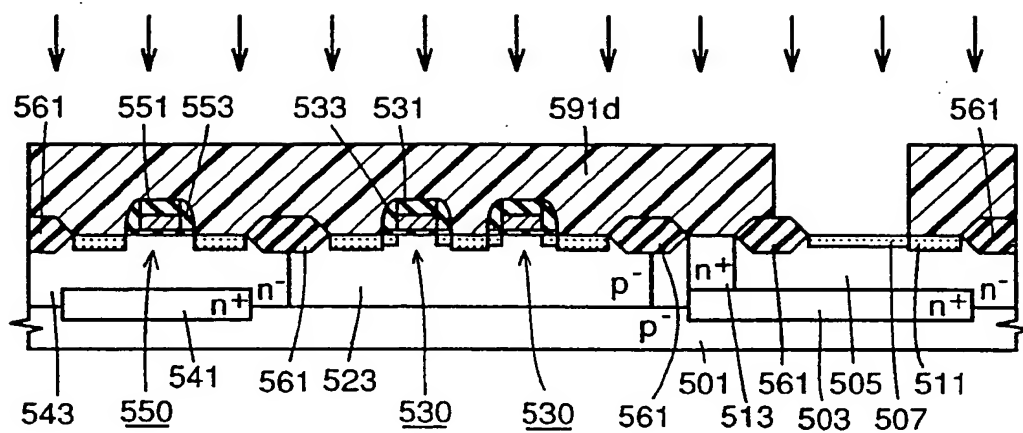


FIG.76

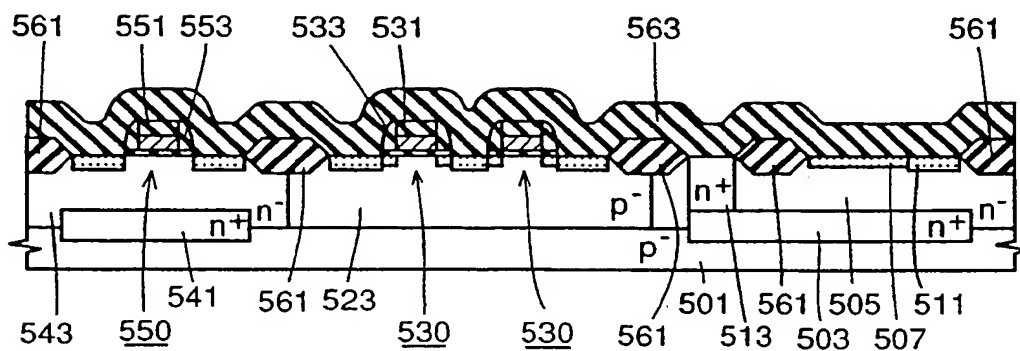


FIG.77

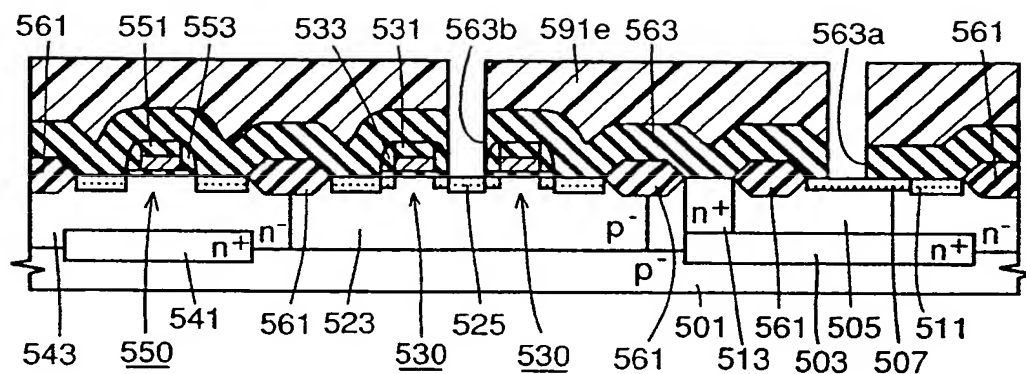


FIG.78

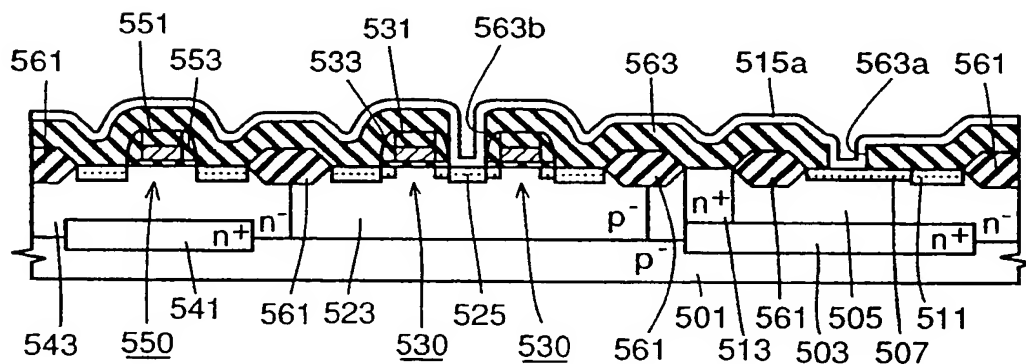


FIG.79

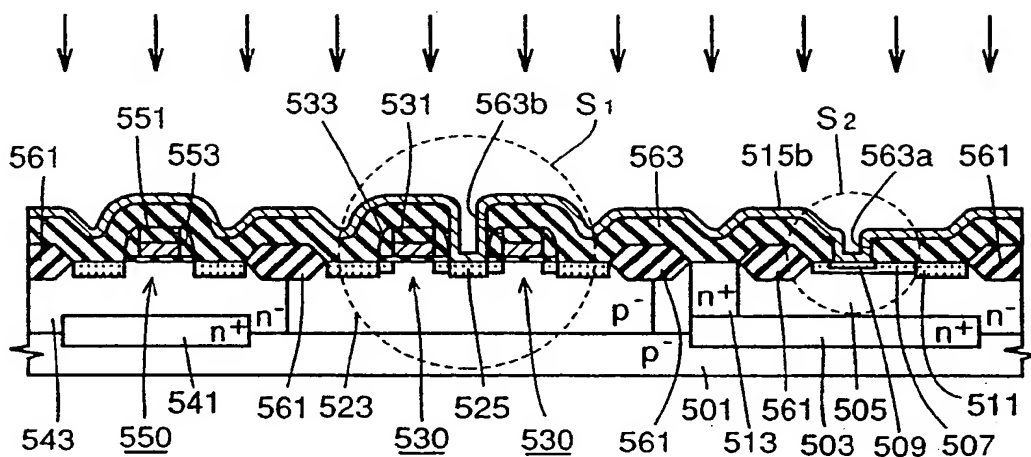


FIG.80

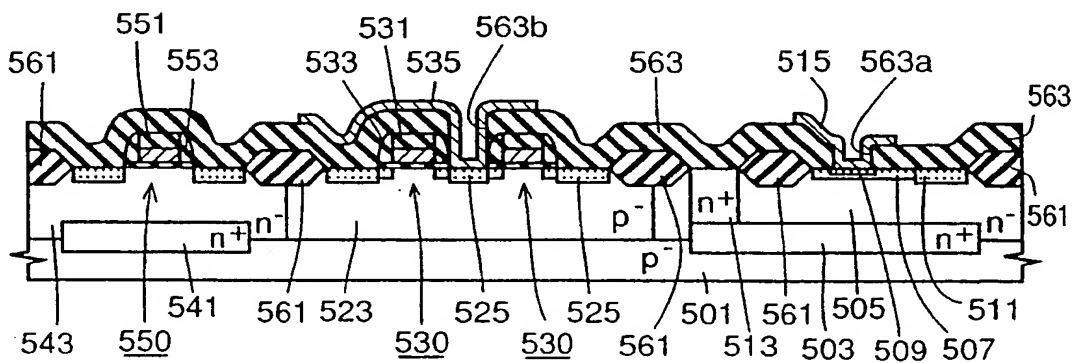


FIG.81

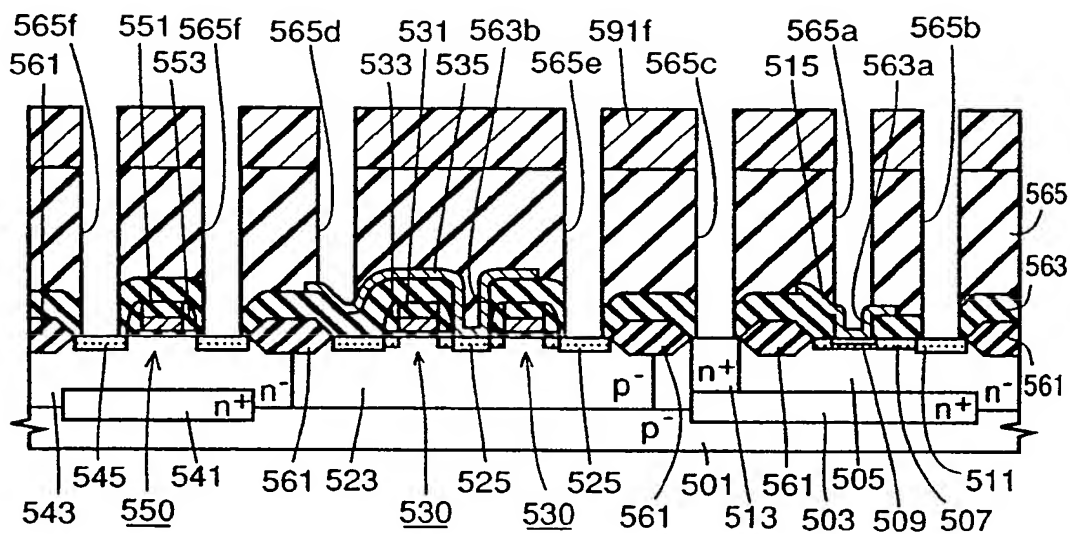


FIG.82

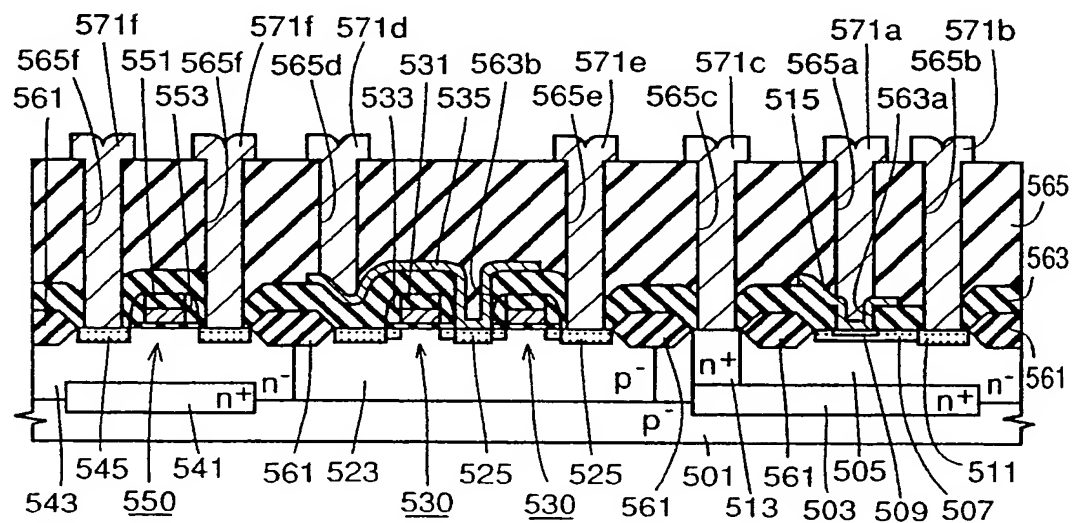




FIG.83

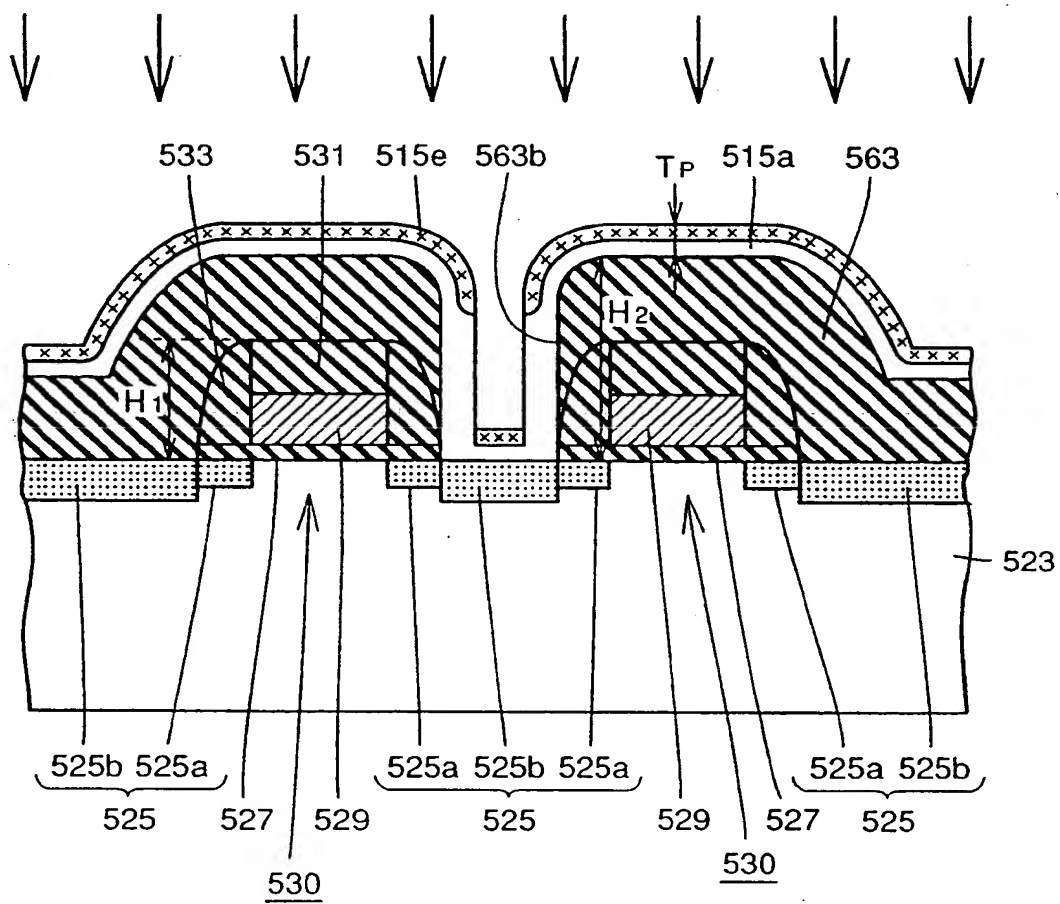


FIG.84

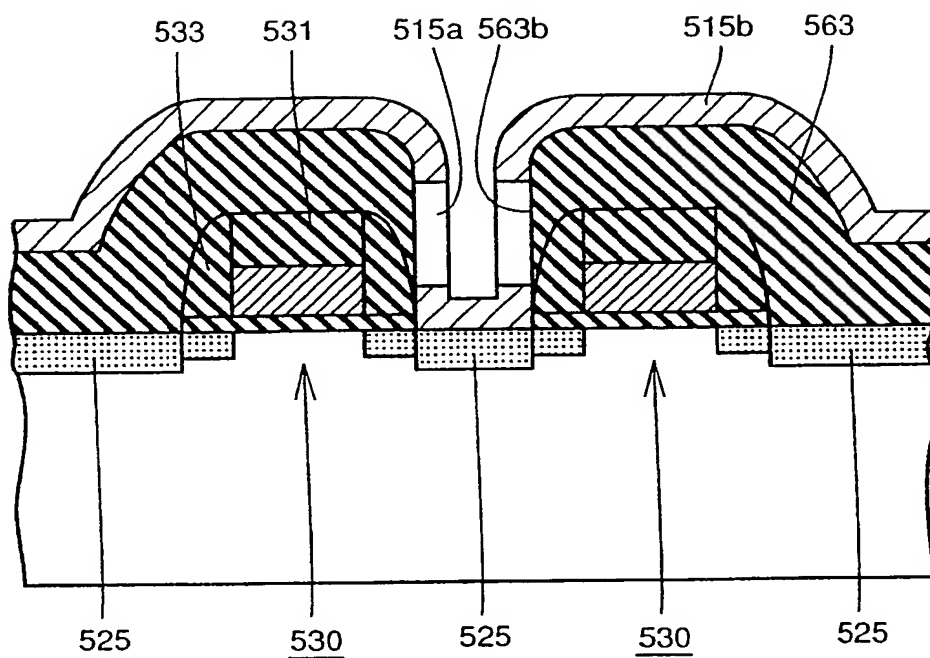


FIG.85

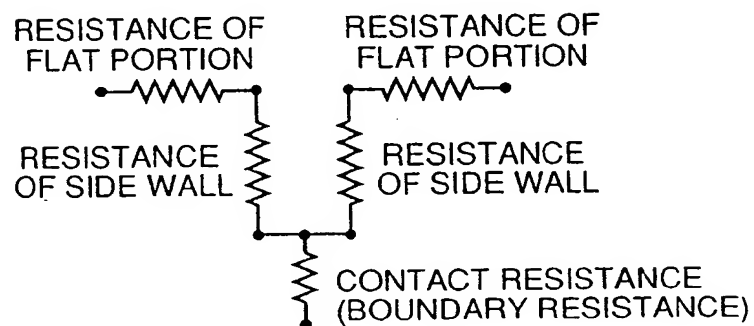


FIG.86

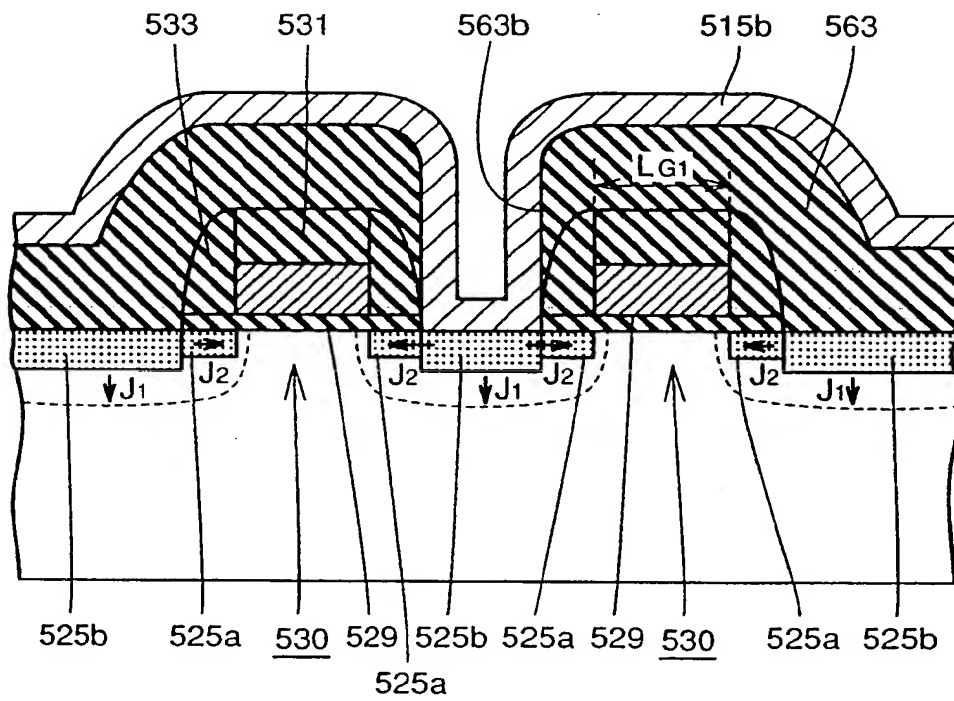


FIG.87

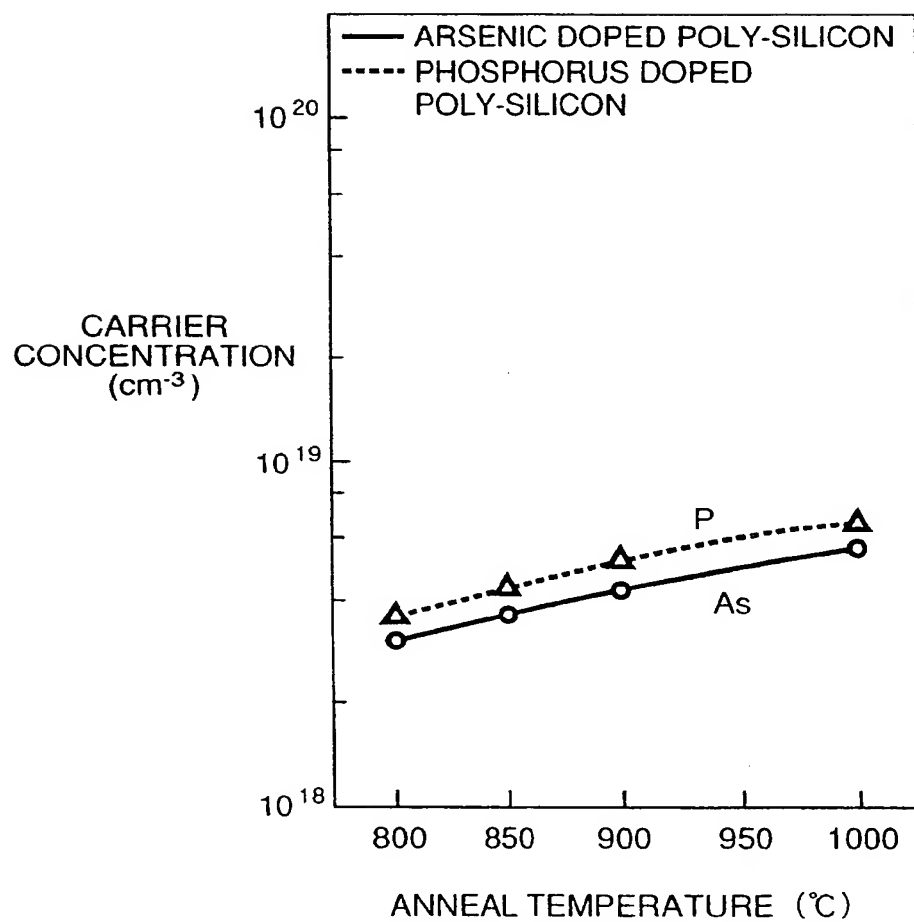


FIG.88

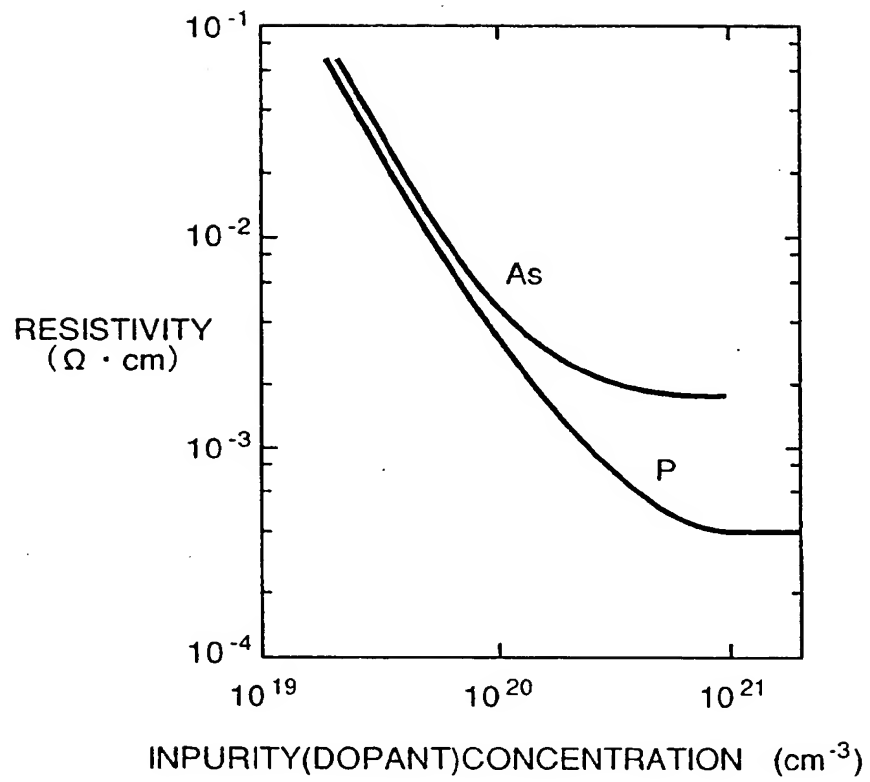
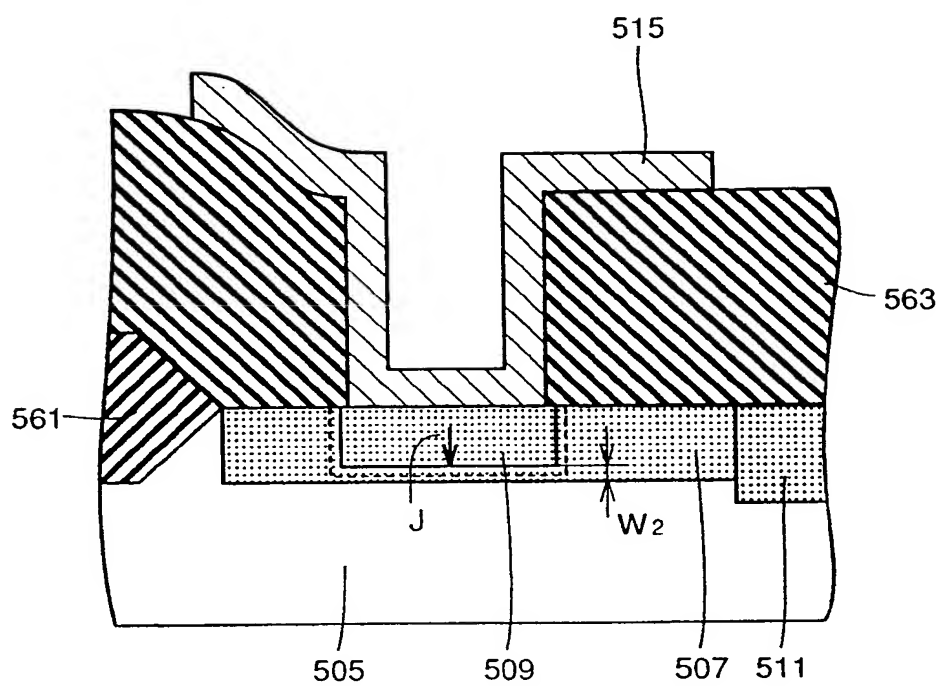


FIG.89



(19)



Europäisches Patentamt  
European Patent Office  
Office européen des brevets



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(51) Int. Cl.<sup>6</sup>: **H01L 21/331, H01L 29/417,  
H01L 21/82, H01L 21/285,  
H01L 29/52**

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(88) Date of deferred publication of the search report:  
**27.12.95 Bulletin 95/52**

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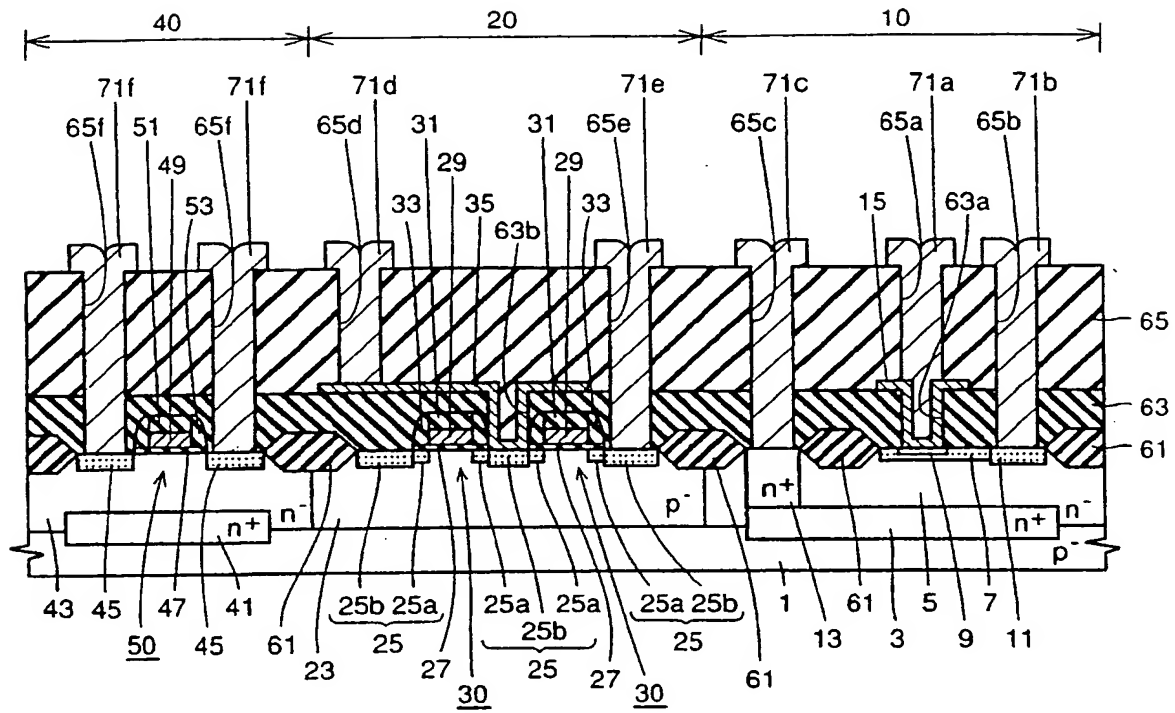
(54) **Semiconductor bipolar device and method of manufacturing the same**

(57) An n<sup>+</sup> buried layer (3) is formed on a surface of p<sup>-</sup> semiconductor substrate (1). An n<sup>-</sup> epitaxial growth layer (5) and an n<sup>+</sup> diffusion layer (13) are formed on a surface of n<sup>+</sup> buried layer (3). A p<sup>-</sup> base region (7) and p<sup>+</sup> external base region (11) adjoining to each other are formed on a surface of

n<sup>-</sup> epitaxial growth layer (5). An n<sup>+</sup> emitter region (9) is formed at a surface of p<sup>-</sup> base region (7). An emitter electrode (15) is formed adjacently to n<sup>+</sup> emitter region (9). Emitter electrode (15) is made of polycrystalline silicon doped with phosphorus at a concentration from 1x10<sup>20</sup>cm<sup>-3</sup> to 6x10<sup>20</sup>cm<sup>-3</sup>.

EP 0 646 952 A3

FIG. 1







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## EUROPEAN SEARCH REPORT

Application Number  
EP 94 11 4761

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	IEEE ELECTRON DEVICE LETTERS, vol.EDL-8, no.7, July 1987 pages 312 - 314 E.P. KEYES ET AL.	1-4,8,9	H01L21/331 H01L29/417 H01L21/82 H01L21/285
Y	* page 312, column 2, paragraph III; figure 1 *	5	
X	EP-A-0 255 882 (SIEMENS) * figures 1,3 *	9,10	
X	EP-A-0 051 500 (FUJITSU)	9-11	
Y	* page 4, line 3 - page 5, line 30; figure 4 *	5	
A	THIN SOLID FILMS, vol.175, no.1, August 1989 pages 43 - 48, XP84268 D. BIELLE-DASPET ET AL. * page 43, paragraph 1 - page 47, paragraph 3 *	9-11	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
<i>The present search report has been drawn up for all claims</i>			
Place of search BERLIN		Date of completion of the search 16 October 1995	Examiner Juhl, A
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 01.82 (P04C01)



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Office

EP 94114761

### CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

### ☒ LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-5,8-11: Polysilicon emitter structure with phosphorous concentration up to  $10^{21} \text{ cm}^{-3}$  and method.
2. Claims 6,7,12,13: Emitter structure with three insulating layers and method.

- ☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respects of which search fees have been paid, namely claims:
- ☒ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims,

namely claims 1-5, 8-11